MODULAR PROCESS CONTROL SYSTEM : A PERSONAL COMPUTER APPROACH

by

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ABSTRACT

Signature

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One of the major uses of personal computers is the process control application to deal with a "real world" environment. The differences between a logic system and control system are isolation, power switching, level translation and noise immunity. In addition, it is desirable to have the I/O devices offer advantages such as :

. configurability

. expandability

. serviceability

. ease of maintenance

. lower design cost

Designing control applications can considerably simplify the effort to map several control functions into a microprocessor's architecture. However, adding multiple control functions to a personal computer architecture can be a problem.

Invidual control functions that must be integrated into a more complex control environment can lose their invidualiity as result.

Considering the commercially available add-ons and add-ins for personal computers in control, measurement, test and monitoring applications, the I/O enhancements dedicate to a single I/O function only. This result is due to the fact that the I/O block for expansion for each computer is limited as is the difference and form of the operating systems of each invidual personal computer.

Although the majority of these products are end-user oriented and not designed into systems for use in control, the field is fast moving and sure to grow. In that light, these peripherals may be specifically designed to operate with a personal computer host in a control environment. The growth in control related add-ons and sophisticated software suggests that the use of a personal computer in a control environment is a reality. One obvious direction in adapting personal computers to data acquisition and control is to network them in a distributed control system. To this end, the popularity of personal computer is most advantageous since it offers tremendous flexibility to a broad spectrum of users in the control application industry.

DESCRIPTORS

DC motors

Direct Digital Control

I/O Driver Interface

Modular Process Control

Stepper Motors

VIC-20

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SCOPE OF THE THESIS

This thesis is a study and implementation of a multiple process control system with the following key elements :

1. Provide the basis for a cost effective implementation of a stand alone process control computer.

2. Provide the configurability to an existing personal computer thus generalizing the application functions.

3. Provide the expandability to the add-ons as a cost effective measures for multiple control applications.

4. Provide coordination for multiple control processes via hardware segmentation to correspond to a modular software implementation.

5. Maintain the invidualíty of each process control element to achieve an independent process to be viewed as a simple control loop.

With these goals, the complexity of a multiple process control system can be simplified and made very useful in a control environment and application.

With the same minimum hardware possible, a VIC-20 and its accessories were chosen as a sample system to develop and to simulate the multiple process control system. The VIC-20 and its accessories are :

1. VIC-20
2. Disk drive or cassette tape (VIC-20 compatible)
3. Printer (VIC-20 compatible)

Besides the VIC-20 and its accessories, additional modular I/O of the system must be included with the specifications described below:

1. <u>D.C.</u> <u>motor</u> <u>driver</u> (see function description and interface specification for information - Appendix B)

2. <u>Swiches,</u> <u>relays</u> (see function description and interface specification - Appendix B)

3. Stepper motor driver (see function description and interface specification for detail - Appendix B)

4. Speed sensing (see function description and interface specification for detail - Appendix B)

5. Input conditioning (see funtion description and interface specification for detail - Appendix B)

1.0 INTRODUCTION

1.1 BACKGROUND

Selection of a particular personal computer for implementing modular process control must consider cost, compatibility and ease of use. In the low cost computer category, it is fairly easy to recognize the COMMODORE 64, VIC-20, ATARI and a number of small computers using the microprocessor 65XX family as their central processors. Whatever the selection of the personal computer in the 65xx family,the I/O expansion should be fairly easy to adapt to the host interconnection. VIC-20 is chosen for its low cost and simple expansion since the I/O block of the VIC-20 already has the output signals and thus making it easy to map directly these I/O modules without having trouble with most of the commercially available software for the VIC-20. On the other hand, for example, COMMODORE 64 doesn't need memory expansion, but it does not dictate the location of the I/O block. Moreover, the COMMODORE uses a bank-switching technique to provide full 64K RAM to be used. This gives the commercially available software to expand the entire range.

The I/O expansion therefore, does not allow direct mapping without causing trouble for the user for certain choices of software. Atari and others also have similar problems. To a certain extent, the problem may not be as serious as it sounds. The user should be able to modify the I/O expansion at the connection to the host and provide a dedicated I/O block in his/her application. Therefore, interfacing with these computers will involve using the 65XX I/O peripherals for compatibility.

The following sections consider the evaluation of the VIC-20 in control applications.

1.2 VIC-20 AND ACCESSORIES

The system will need the following devices to perform as stand alone controller :

1. VIC-20 as the central processor for the system.

2. Disk drive for floppy diskettes or data cassette recorder for cassette tape for storage.

3. Printer for hard copy or outstanding data logging.

1.3 MEMORY MAP AND I/O FACILITY

1.3.1 VIC USER MEMORY

The VIC-20 memory map in Figure 1 gives the general configuration of facilities with dedicated I/O and possible expansion.

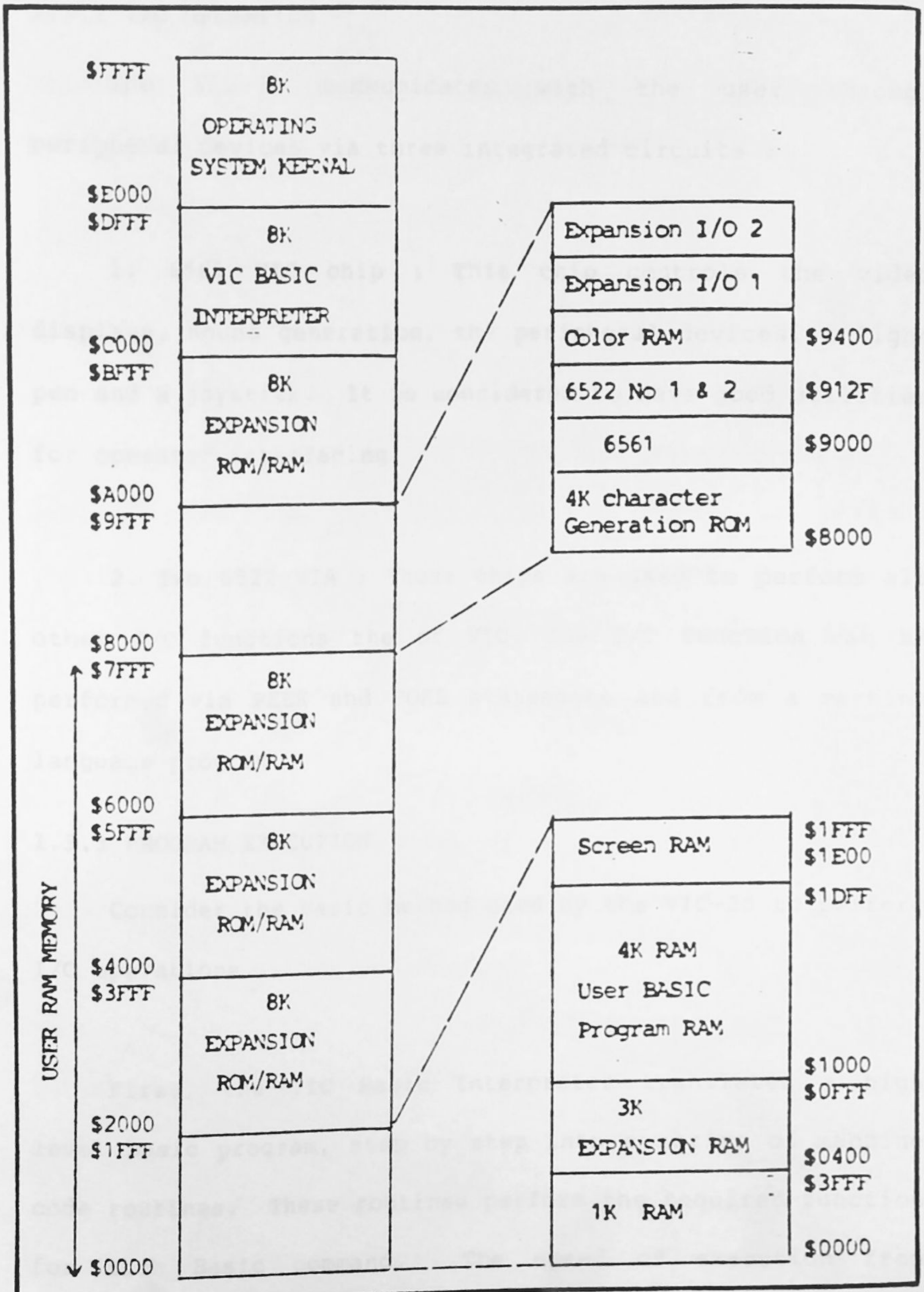


Figure 1 : VIC-20 MEMORY MAP

1.3.2 I/O OPERATION

The VIC-20 communicates with the user through peripheral devices via three integrated circuits :

1. 6561 VIC chip : This chip controls the video displays, sound generation, the peripheral devices, a light pen and a joystick. It is considered to have good utilities for operator interfacing.

2. Two 6522 VIA : Those chips are used to perform all other I/O functions the of VIC. The I/O function can be performed via PEEK and POKE statements and from a machine language program.

1.3.3 PROGRAM EXECUTION

Consider the basic method used by the VIC-20 to perform I/O operations.

First, the VIC Basic Interpreter translates a high level basic program, step by step into a series of machine code routines. These routines perform the required function for each Basic command. The speed of execution from

interpretted Basic will be slow compared to compiled and assembled machine code and there is no mechanism for multitasking.

Second, the VIC can be programmed in both Basic and machine code via USR and SYS. Variables can be transferred between a Basic program and a machine code program by using PEEK and POKE. This makes it possible to develop an I/O driver which can intercept the interrupt to perform multitasking via the interpreter without a separate development system. I/O machine code routines can be developed to enhance the I/O control functions.

1.3.4 SPEED

The speed of execution of the VIC-20 is the most important factor in the proposed system since it will restrain the system to a certain rate of sampling of operation as well as special application. A trade off must be considered between fast operation and possible I/O expansion. A trade off is also considered in programming with multitasking requirements between the dedicated I/O machine language routines and transfer of data to the

interpretive Basic. An alternative to this is an I/O kernel and a compiler language to speed up the extension and achieve multitasking. For further information, see " A VIC-20 COMPILER FOR CONTROL SYSTEM " which is written by Oanh Kim Ngoc Huynh as a Master of Science Thesis, UNIVERSITY OF PITTSBURGH (1985).

2.0 MODULAR PROCESS CONTROL

Before beginning the design, let us consider an overview of the general process control function and its attributes. Process control involves :

1. centralized control of multiple actions such as "global" decision making ability.

2. decisions, which must be translated into actions such as the I/O driver's ability to perform a given task.

3. tasks, these can be categorized in specific dedicated functions as execution of routines or subroutines.

2.1 DIRECT DIGITAL CONTROL

Using the personal computer in process control can be seen as applying direct digital control in control technology. Direct digital control replaces process control which traditionally has proved to be pneumatic, analog and

other devices. The principal disadvantage of systems based on the old technology is that their components are difficult to adjust and require high levels of maintenance due to such things as wear and deterioration.

Direct digital control on the other hand provides quick, accurate and consistent responses. If the adjustments are necessary, they can be made from the operator keyboard. The direct digital control also provides the following features which are inherent :

- maintaining a body of knowledge about the overall system

- collecting information from multiple inputs

- implementing a built-in automation function

- recognizing and reacting to exceptional operating conditions

- excecuting routines and performing overall supervision

2.1.1 SPEED CONTROL

The direct digital control has to deal with different types of control applications. The most obvious one is speed control of a motor. The variable speed motors are most common in today's control applications. Whether constant torque control, constant speed control, acceleration, deceleration control or just simply variable voltage control during start up to avoid the motor burning out, these applications have one thing in common : a variable voltage is applied to a motor, based on that motor's condition (i.e. speed, torque, current) and an external control setting. Although there are several types of D.C. motors, only the most common of these requiring a single power supply are considered here. In many cases, the purpose of the controller is to maintain the speed required for process variations such as temperature, speed, current and load which is supplied to the controller in digital form by several techniques. The speed of the motor therefore can be regulated via a voltage level to the driver or amplifier circuit. The control algorithm may be a single type or a combination of types, e.g., proportional, integral and differential. Application of this type will offer

flexibility by making available inexpensive computer peripherals such as disk drives and printers as well as providing automation.

2.1.2 DIGITAL MOTION CONTROL

The direct digital control is also taking in digital motion control. The digital motion control application is important to process control. It is easier to control the characteristics of the system stability and motion by programming rather than by changes in analog components. These applications range from computer peripherals such as disk drives and printers to automation and robotics.

The traditional closed loop analog servo systems are gradually being replaced by microstepping motors. The multi-axis control gains well founded in factory automation and robotics with the key elements being the position-control system - the stepping motor. The popularity of the stepping motor is steadily increasing along with its controller. The higher level controlers add intelligence and other features make modularization of a system a lot easier. Similar improvements in quality stepping motors thus simplify

digital motion control into what is evolving as a universal stepping motor controller. Multi-axis control of up to 8 separate devices can be implemented to provide synchronization in robotics.

2.1.3 DATA ACQUISITION

Direct digital control also involves data acquisition from multiple resources. Data acquisition plays an active role in providing the process variable inputs as well as status variable inputs.

The information gathered from the process and from the operations is available for control strategies, condition, displays and reports. An important consideration for refining a process is the ability to grow easily as the plan expands or as the new applications are developed. Equally important is the flexibility of the system in adapting to changing requirements as control techniques are improved. The key elements of data acquisition are speed and accuracy. These elements can dictate the limitation on a particular form of process control. Additionally, the data acquisition module depends on the speed of the processor as well for systems without coprocessors.

2.1.4 BINARY I/O CONTROL

Direct digital control can be as simple as binary I/O control. Generally, the binary I/O control is involved in ON/OFF control or digitally sensing a set of time or positional attributes. In fact, binary I/O control also is involved in time-proportioning control by modulation of the on-time of a motor in chopper driver applications. It is also involved in the position-proportioning control by performing modulation of the on-time of a bidirectional motor, based on the full travel time of the motor between two extremes. The key elements in this type of control are isolation and voltage level translation.

2.2 REAL TIME CONTROL

Process control also deals with the "real world". To deal with the "real world" is the function of a real time control systems.

The most difficult decisions often made in dealing with real time control systems are involved with architectural

issues. The architecture of a system is the general scheme of the organization, behavior and function of a computer. In chosing a personal computer to perform a real time control application, the I/O hardware may or may not bring to fruition all the inherent benefits of a specific architecture. This is because the speed at which real time applications run is dependent on the design efficiency of the I/O implementation.

2.2.1 TIME CONSTRAINTS

Real time control imposes several constraints but the most obvious one is time. The time constraints are those related to the funtionality of a CPU to a device interface. They are both hardware and software dependent and characterized by a minimum of user interaction. In a closed-loop control application, the response time of the process control must be met. In motion control, application of the stepping rate or acceleration rate must be met. The evaluation of the hardware approach and the software approach is required before implementing the system.

2.2.2 SYNCHRONIZATION

Real time control is also involved in synchronizing several functions to perform an unique control function. As mentioned in a multi-axis robotic application, certain motion control must be applied synchronously to multiple devices. The I/O implementation of this type of the control must be flexible enough to allow a simple modular software approach to succeed.

2.2.3 MULTITASKING

Process control is making a "global" decision of the whole process which may consist of many tasks that are required to be performed in coordination with each other. The software that directs a real time control system is primarily concerned with monitoring and controlling devices. They are for the most part much slower than the main processor. It is possible to respond to each device in a timely manner with multitasking. Perhaps the most important characteristics of real time software are responsiveness and multitasking. Moreover, the viable means for multitasking to succeed is the device-generated interrupts. The system is even said to be interrupt-driven. The software now can

handle many task concurrently, since in the real world, events generally overlap each other. Implementing a system or architecture requires certain hardware involvement without limiting the I/O operations to the use of contiguous addressable I/O devices will enhance this particular application.

2.3 MODULARITY

The previous discussion defined the type of the control functions and its attributes. To achieve a cost-effective design, we must evaluate the objectives of the modularization.

Considering all of the benefits of modularization is the evaluation of the system from the standpoint of flexibility in the following areas :

- configurability

- expandability

- controllability

2.3.1 CONFIGURABILITY

The modular structure is configurable : a user can select a set of I/O modules and organize to his/her need to minimize the extra cost. In addition, as the application requires certain changes in I/O requirements, the user can simply reorganize the I/O modules or add more to an existing system with an additional module. This prevents the cost of re-establishing a new system.

2.3.2 EXPANDABILITY

The modular structure is expandable : a user can upgrade a system by adding more cluster (I/O bus expansion modules) to an entry system at the price of additional modules. The key expansion elements are the addressability and power consumption. For the VIC-20, the I/O block provides a range for I/O expansion. The power consumption is stackable since separate power requirements are met by separate supplies. Isolation is also provided.

2.3.3 CONTROLLABILITY

This is of question implementation. The algorithms of digital control systems are quickly overtaking analog controllers. Designers must understand that using a microprocessor does not solve all design problems. The limitations are also numerous such as finite word length, A/D and D/A resolution, speed and accuracy of computation. These deficiencies can be analyzed prior to configuring a system to avoid adverse effects on the stability of the closed-loop systems.

2.4 PROGRAMABILITY

In addition to lowering the cost, the design objective must be directed to how easy the programming phase will be. If the modularity has a strong basis for the hardware implementation of a process control system, the programability also has a strong basis for the user interface and software development.

Let us take a look at a few requirements :

2.4.1 DATA LOGGING AND DISPLAY

The peripherals of a personal computer usually offer a variety of the input and output support as well as storage. However, many applications are required to use the large storage capability while the others may require a high resolution display. In the scope of this thesis, we can see that the VIC-20 provides limited expansion in terms of the storage and display. The evaluation of this type of control should be considered if large amounts of storage or high resolution display is needed.

2.4.2 DATA MANIPULATION

Generally, the I/O interface can dictate the data structure. Not only the resolution and accuracy, but also the polarity and range in which the data can be used. The uniqueness of each process control function of similar I/O device must be considered. This characteristic is often confused with the software issue but in fact, it is an architectural requirement.

2.4.3 COMPUTATION

Computability may be the broadest issue to be deal with in the personal computer. However, the user can not ignore the problem that he or she has to be able to ensure the accuracy of any computation. In general, the personal computer can not satisfy the number crunching capability of many highly complex functions.

3.0 SYSTEM OVERVIEW

3.1 SYSTEM ARCHITECTURE

In a modular process control application, the user decides the hardware configuration to the outset of the design. Selecting proper hardware and language to evaluate the performance of the system is an important problem. At this time, the user must pay special attention to the hardware configuration of the system as a whole for connecting or installing I/O interfaces. From a programming standpoint, the hardware segmentation corresponds to modular software helping the user to executing a program effectively. Each I/O interface serves as the fundamental unit used for similar functions. The processor deals with a segment through a consistent data structure which simplifies the software writing for dissimilar routines.

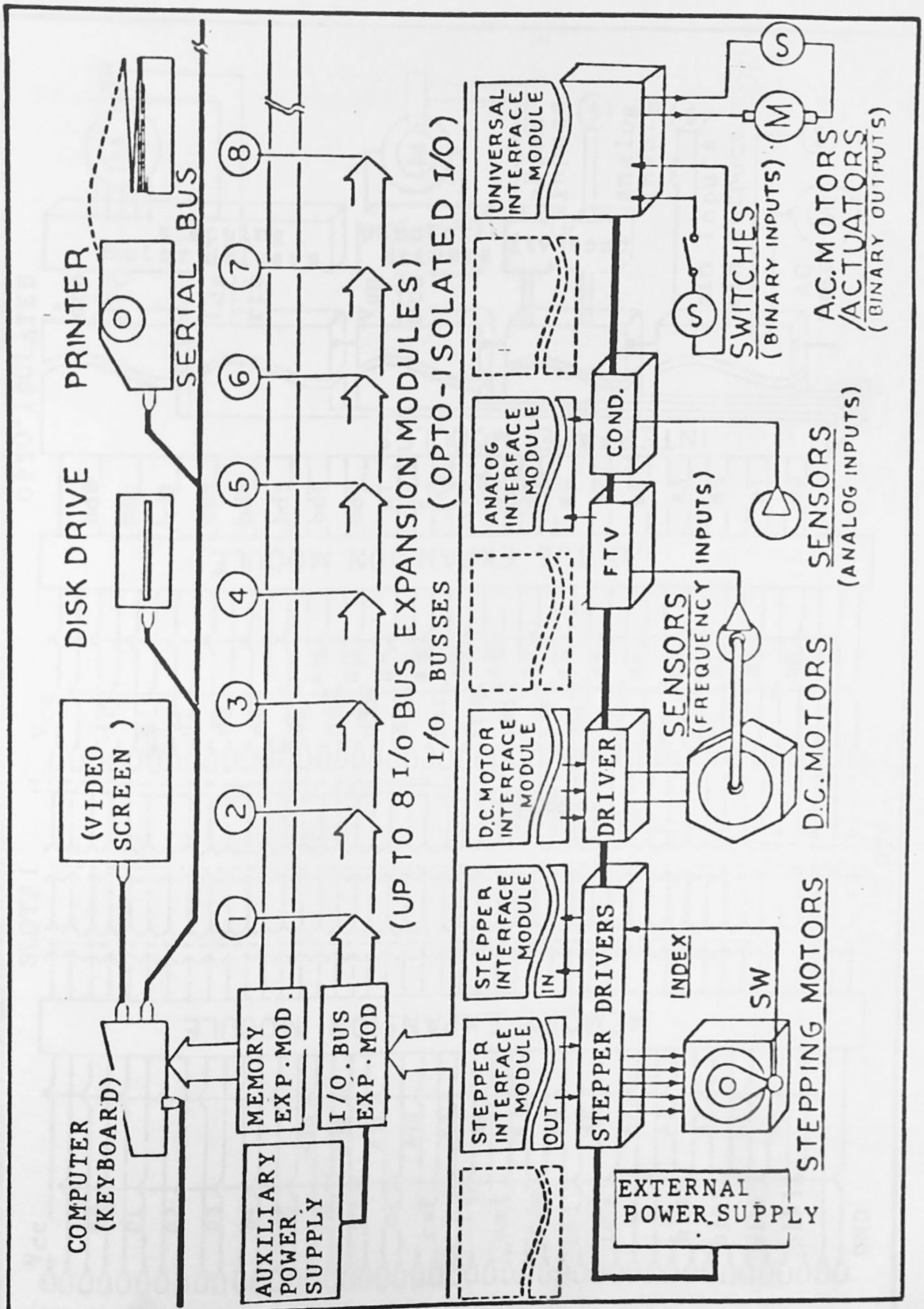


Figure 2 : SYSTEM ARCHITECTURE

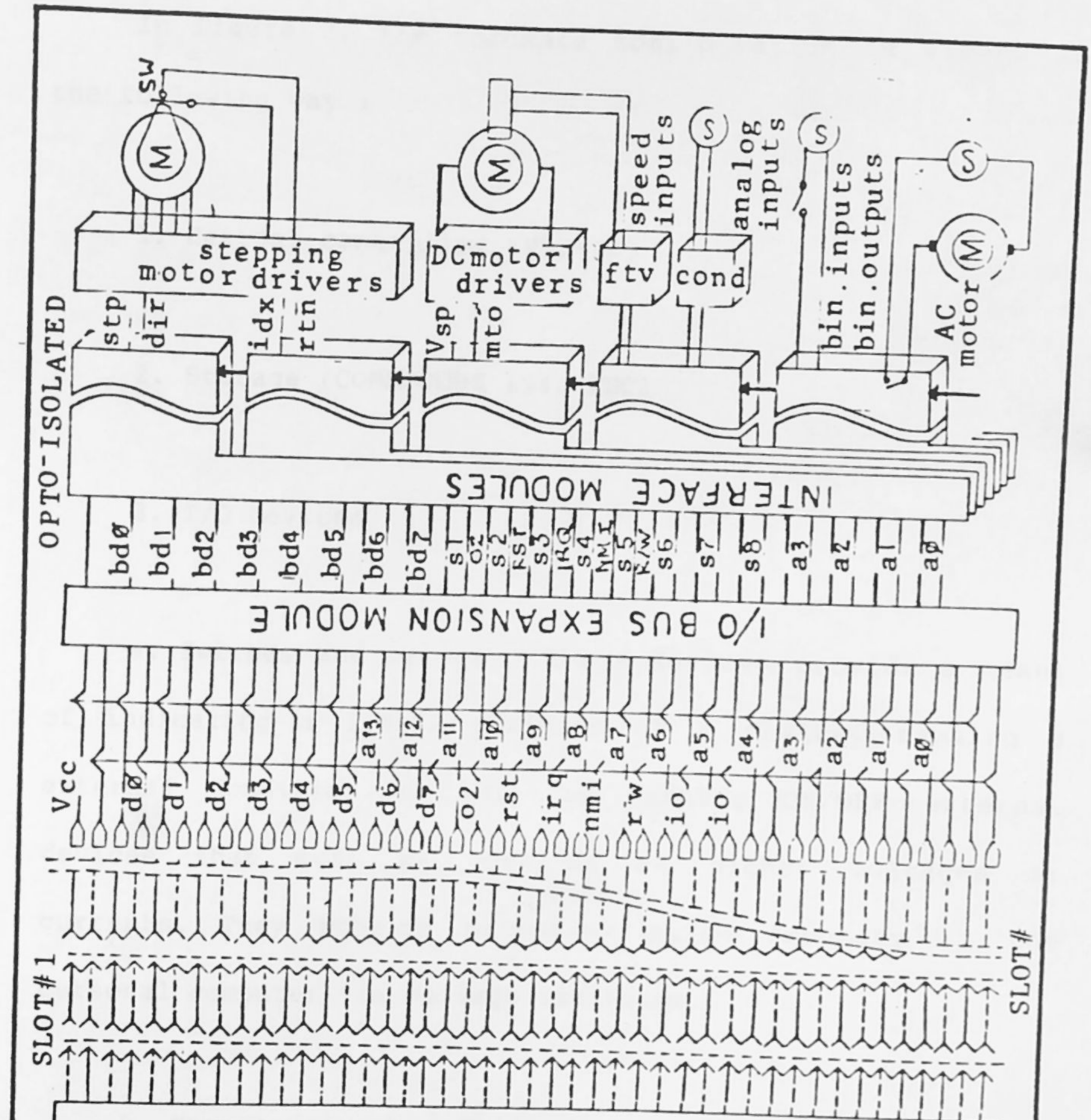


Figure 3 : SYSTEM INTERFACE CONNECTION

In Figure 2, the hardware configuration is viewed in the following way :

1. Central controller (VIC-20)

2. Storage (COMMODORE 1541 FDC)

3. I/O Devices

a. Swiches and relays : These devices provide a means of indicating a limit, position of a device, sensing a external condition as well as turning ON/OFF external devices that must be operated at higher voltages or currents. They provide necessary noise immunity to the personal computer via voltage isolation.

b. Stepper motors : These devices are used to position a mechanical instrument or a pneumatic device. A pair of two motors may be interpreted as X-Y positioning device. Multiple sets of stepper motors can be used to achieve a complex motion. These devices can be mechanically indexed to provide a simple zeroing motion or to restore the original

position of the system. Direction is also used to enhance these features.

c. D.C. motors : In speed control applications, these devices can be configured as a closed-loop with some number of bits resolution. The actual speed can be set to certain value. The motor can be turned ON/OFF at the user command.

3.2 MODULAR APPROACH

Providing the basis for a cost effective implementation of a process control system is to provide maximum flexibility via modularization. However, the modularity can be perceived in many different ways.

In one case, the dedicated I/O processor can be networked to a host as in say a distributed control system. In another case, the add-on I/O interface to an existing processor can broaden the range of a stand alone controller. This thesis proposes the add-on I/O interface as a short range solution by adapting the personal computer to be a configurable I/O processor and further suggests that this I/O processor can be networked in the distributed control system as well. The modular approach can be interpreted as an hardware implementation of a configurable I/O interface structure to convert a personal computer into a single I/O processor

3.2.1 BUS STRUCTURE

The I/O expansion from the existing architecture of a personal computer will involve examining the memory map and the bus structure. The VIC-20 and similar 65XX-based personal computers use memory mapped I/O. The standard interfaces usually are 652X series which directly connect to the data bus, address bus, control lines. The I/O expansion for a 65XX-based personal computer simply means attaching the 652X to this bus. The addressable range of this device can be seen as a decoding problem. As for the VIC-20, the I/O expansion ranges from $9800 to $9FFF which can provide the expansion up to 64 of the 652X-type devices. Breaking 64 devices into 8 sets of 8 is essentially providing an I/O bus to accommodate the connecting facility. In order for a full expansion to be realized, each cluster (I/O bus expansion module) must be capable of supporting itself via paralleling the power supply. In addition, the I/O buses must be buffered.

3.2.2 FUNCTION PARTITIONING

As mentioned earlier, the modular expansion can be centered around a cluster of the 8 I/O interfaces. Eight 6522's can provide 8 different I/O interfaces modules. Typically, this could be the binary inputs, binary outputs, analog inputs, analog outputs or the combination of any two dependent on the application. The connection of these interface modules is by means of I/O buses.

3.2.3 ADDRESSABILITY

For programming convenience, the 8 clusters can be programmed hardwarewise via mini-jumpers thus providing the user the ability to select an I/O block for I/O expansion while attaching the personal computer to other add-ons. The addressability also provides the convenience for different personal computers to connect to the I/O interfaces.

3.3 I/O APPROACH

Consider a process control of DC voltages as an application which requires a mixture of these devices including those involving AC voltage.

3.3.1 DC AND AC PARAMETERS

The input and output voltages of the external devices are often the most critical parameters. Providing a good range of variation in terms of the input and output voltages requires the selection of component. The interface specification in Appendix B provides the user with the most often needed information.

3.3.2 VOLTAGE ISOLATION

Noise immunity requires good grounding, decoupling and voltage isolation. Since I/O devices are generally operating at high voltage which may cause large transients to disrupt the control operation. The user must follow the interface specification to select the proper interface module.

3.4 SOFTWARE APPROACH

The task of providing the relationships between the various system components falls into the category of writing the software. Before actually beginning to develop software, we will define certain guidelines which can be used to organize and simplify the tasks.

First, consider the environment under which the program will operate. Essentially, there are two choices :

1. Consider the entire process as a sequence of separate operations (i.e. single process).

2. Consider entire process as a set of concurrent operations (i.e. multitasking process).

Second, consider the language which will be used to actually define the required operation. The use of the language will affect the environment as well as speed of the operations. There are several choices :

1. Machine language - which probably is the most flexible and fast but the most difficult to use

2. Interpreted language - which may pose a problem for multitasking and speed

3. Compiled language - which may not be available with the I/O kernel to perform the I/O function since it is machine dependent.

Third, the software implementation can begin as soon as we have broken our control functions into independent "tasks". Then we can handle each separately or have it communicate or be interlocked with another. With this in mind, we can begin the task of actually generating the code which will complete our applications and provide an operating system.

4.0 IMPLEMENTATION

4.1 INTERFACES MODULES

Modular structure can be implemented in the simple form of a bus structure. The VIC-20 expansion port provides access to the data bus, address bus and control signals. However, the VIC-20 can not support full bus expansion. The I/O bus expansion is derived from the VIC-20 expansion with its external power supply, fully buffered bus and addressable I/O interface.

Figure 4 shows the memory expansion module. The module provides up to 24 k of RAM memory and 8 K of EPROM to be expanded. It also provides the facility as a back plane for I/O buses.

Figure 5 shows the detail of the I/O bus. The I/O bus configured as a back plane for 8 I/O interface modules

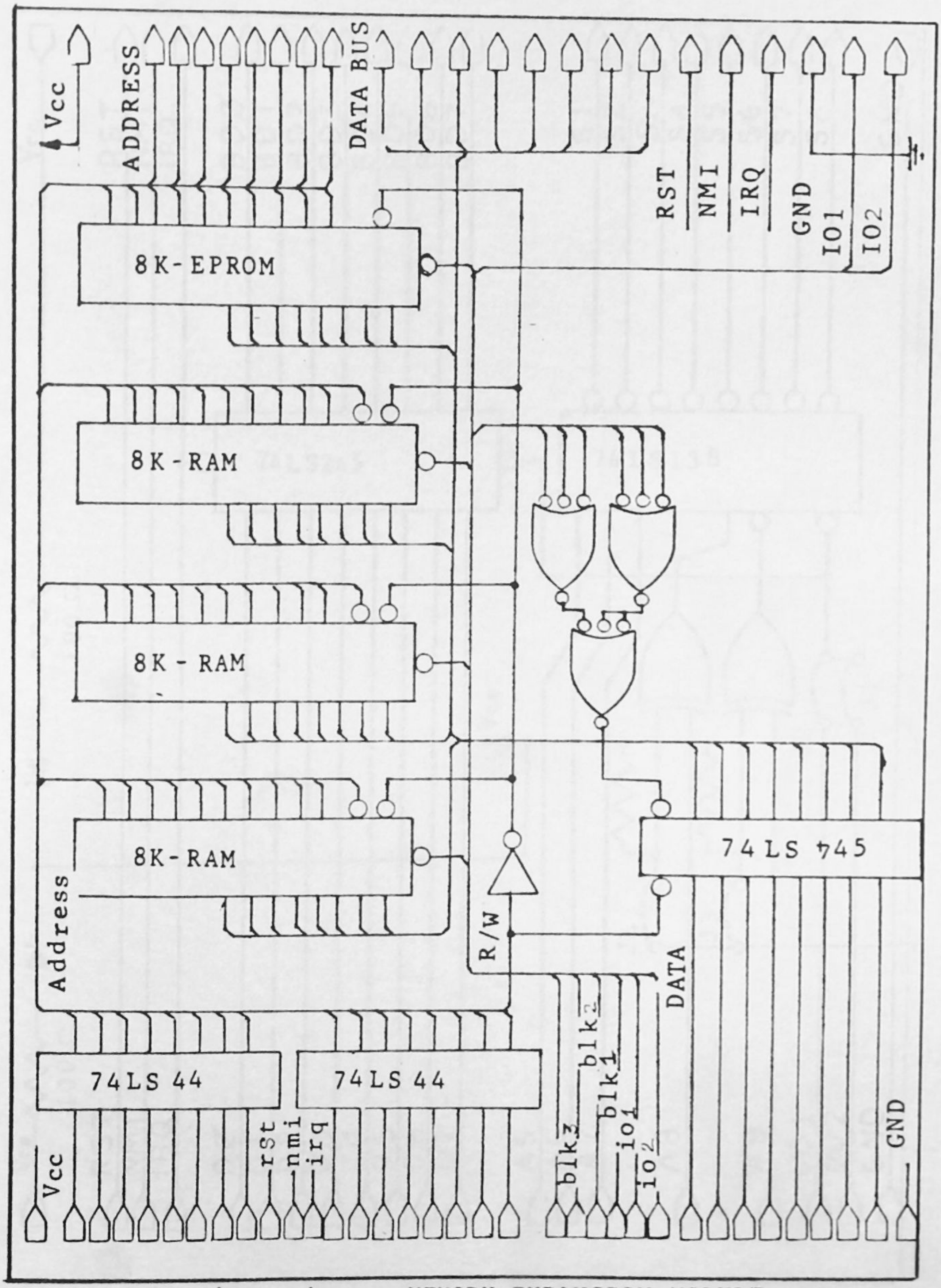


Figure 4 : MEMORY EXPANSION MODULE

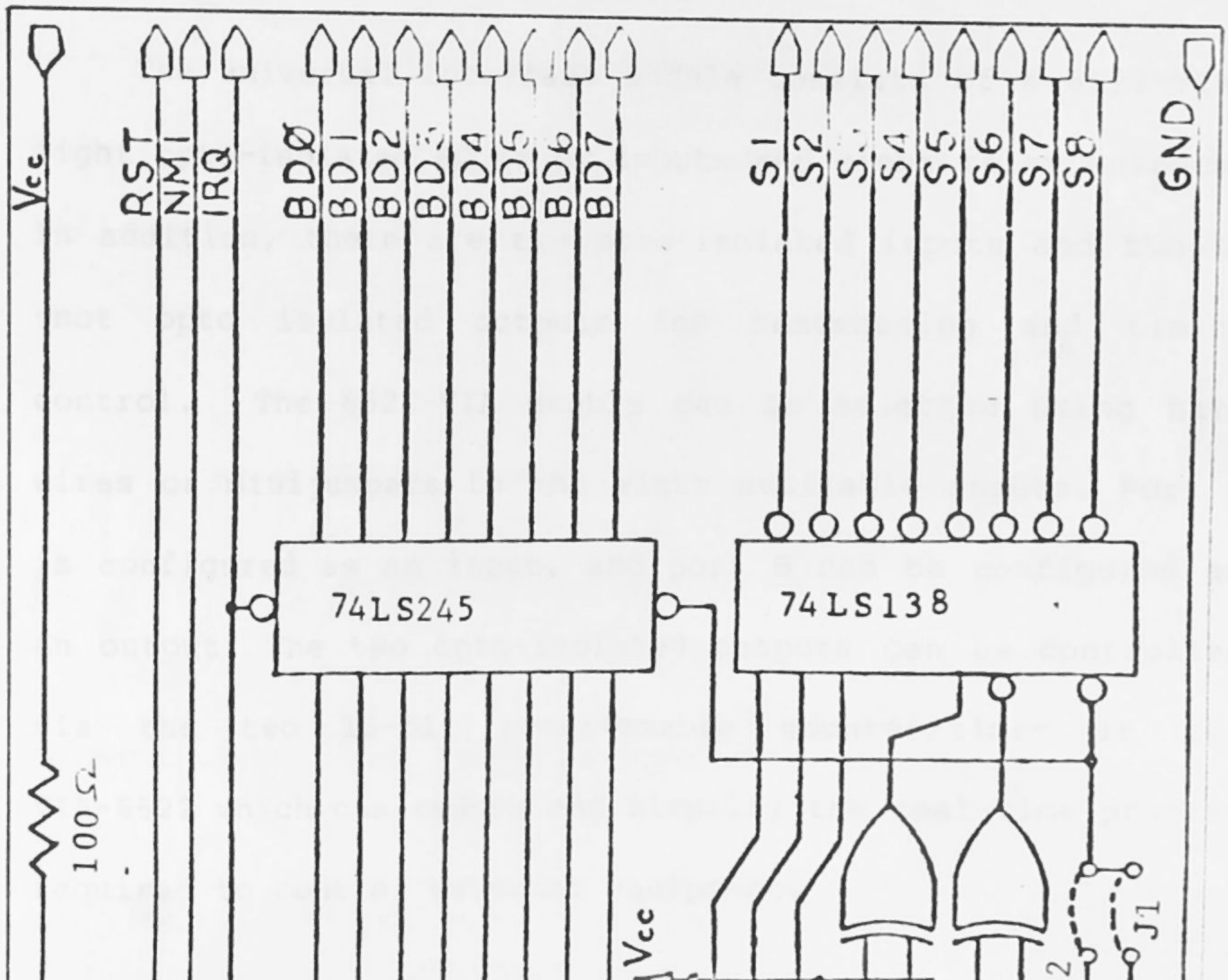


Figure 5 : I/O BUS SPECIFICATIONS

4.1.1 UNIVERSAL INTERFACE MODULES

The universal interface module consists of a 6522-VIA, eight opto-isolated AC or DC inputs and eight relay outputs. In addition, there are two opto-isolated inputs and two 1-shot opto isolated outputs for handshaking and timing control. The 6522-VIA enable can be selected using hard wires or minijumpers to the eight available inputs. Port A is configured as an input, and port B can be configured as an output. The two opto-isolated outputs can be controlled via the two 16-bit programmable counter/timer in the VIA-6522 which can reduce and simplify the real-time program required to control external equipment.

Figure 6 shows the detail of the interface circuit. The interface is intended for an ON/OFF control application. However, time-proportioning or position-proportioning control can be also applied.

The eight opto-isolated AC or DC inputs have a wide range of voltage and current inputs which will allow a large number of control applications such as temperature control, AC line detection, switch closure detection, etc.

The eight outputs have the capacity to switch a large AC or DC voltage and current which can be used to control a medium size motor and a variety of appliances. These relays are protected with slow blow fuses and transorbs for an inductive load.

For programming detail, please refer to Appendix A.

4.1.2 STEPPING MOTOR CONTROL INTERFACES (OUTPUTS)

The interface consists of a 6522-VIA, 16 opto-isolated outputs, one 1-shot opto-isolated output, eight two-input NAND gates, one inverter and discretes. Both port A and port B on the VIA are configured as outputs to provide direction control on port A and step control on port B. The opto-isolated outputs from port B are gated with the 1-shot output to produce 8 step control outputs. This arrangement allows synchronization of up to 8 stepping motors to form complex motion control with simple control by the software. The 1-shot output timing can be adjusted to the timing requirement of the stepping motor driver. This interface alone will be sufficient to control the stepping motor. In conjunction with the circuit described in section 4.1.3

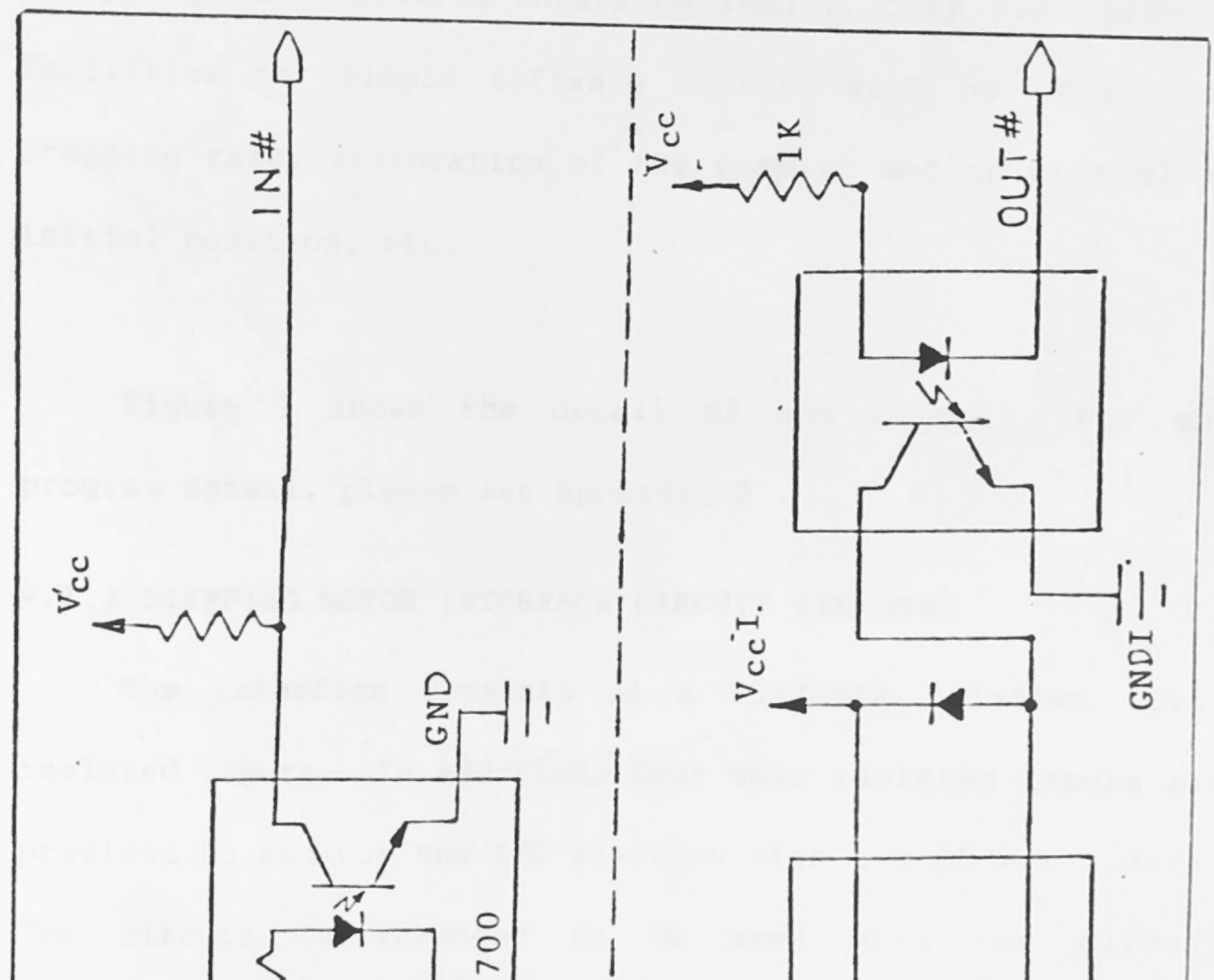


Figure 6 : UNIVERSAL INTERFACE CIRCUIT

(Stepping motor control interface input), they will provide facilities for simple software control such as selectable stepping rate, restoration of the complex motion control to initial position, etc.

Figure 7 shows the detail of the circuit. For the program detail, please see Appendix A .

4.1.3 STEPPING MOTOR INTERFACE CIRCUIT (INPUTS)

The interface consists of a 6522-VIA, sixteen opto-isolated inputs. In addition, four opto-isolated inputs are provided to enhance the I/O function with two 16-bit timers. The circuit is intended to be used with the circuit described in section 4.1.2 (Stepping Motor Control Interface Circuit - outputs -) to provide the status of the 8 stepping motors with different stepping rate requirements. However, the interface can be used as the DC low voltage binary inputs such as switch closures, position sensing, etc.

Figure 8 shows the detail of the circuit. For programming detail, please see Appendix A.

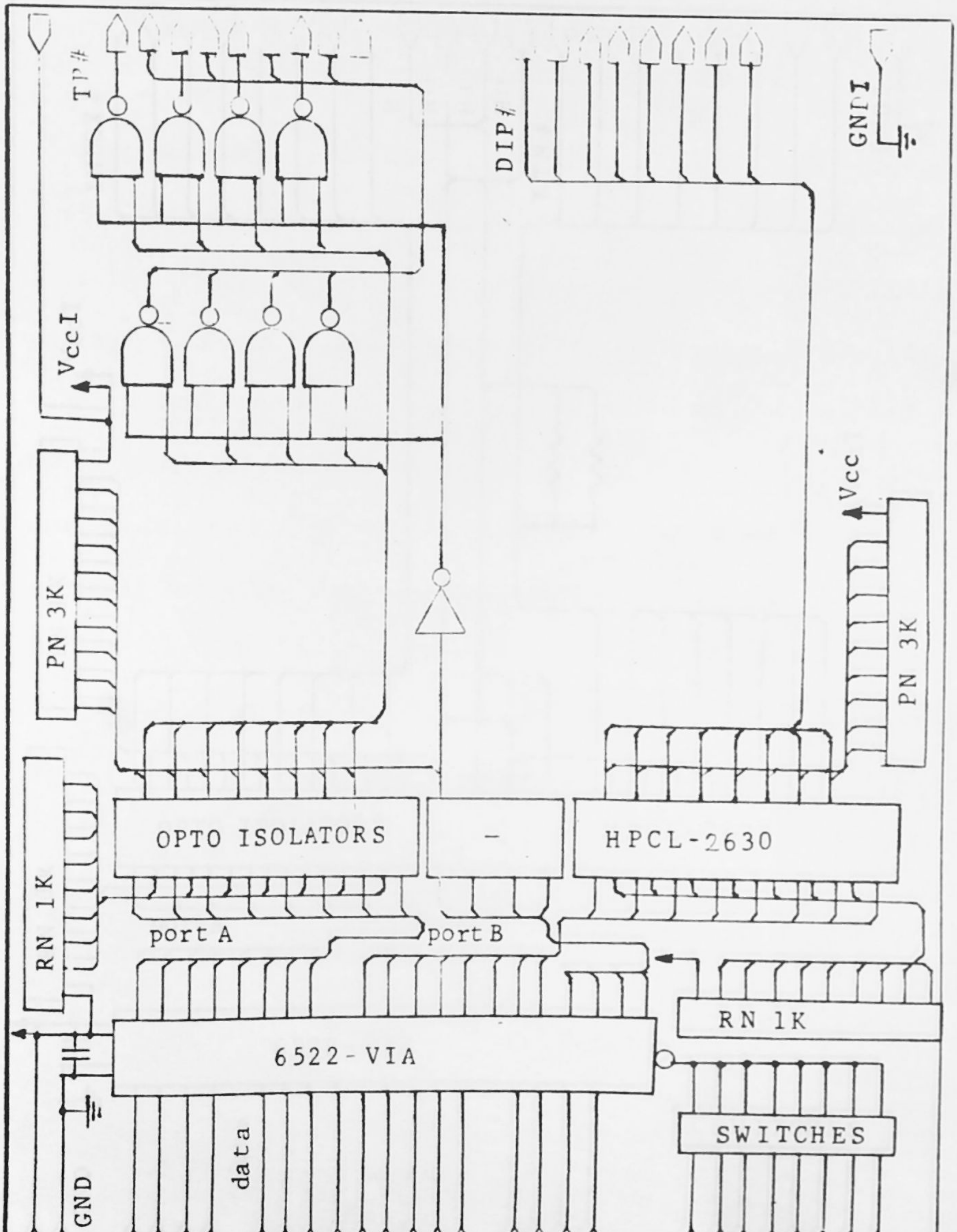


Figure 7 : STEPPING MOTOR INTERFACE CIRCUIT (OUTPUTS)

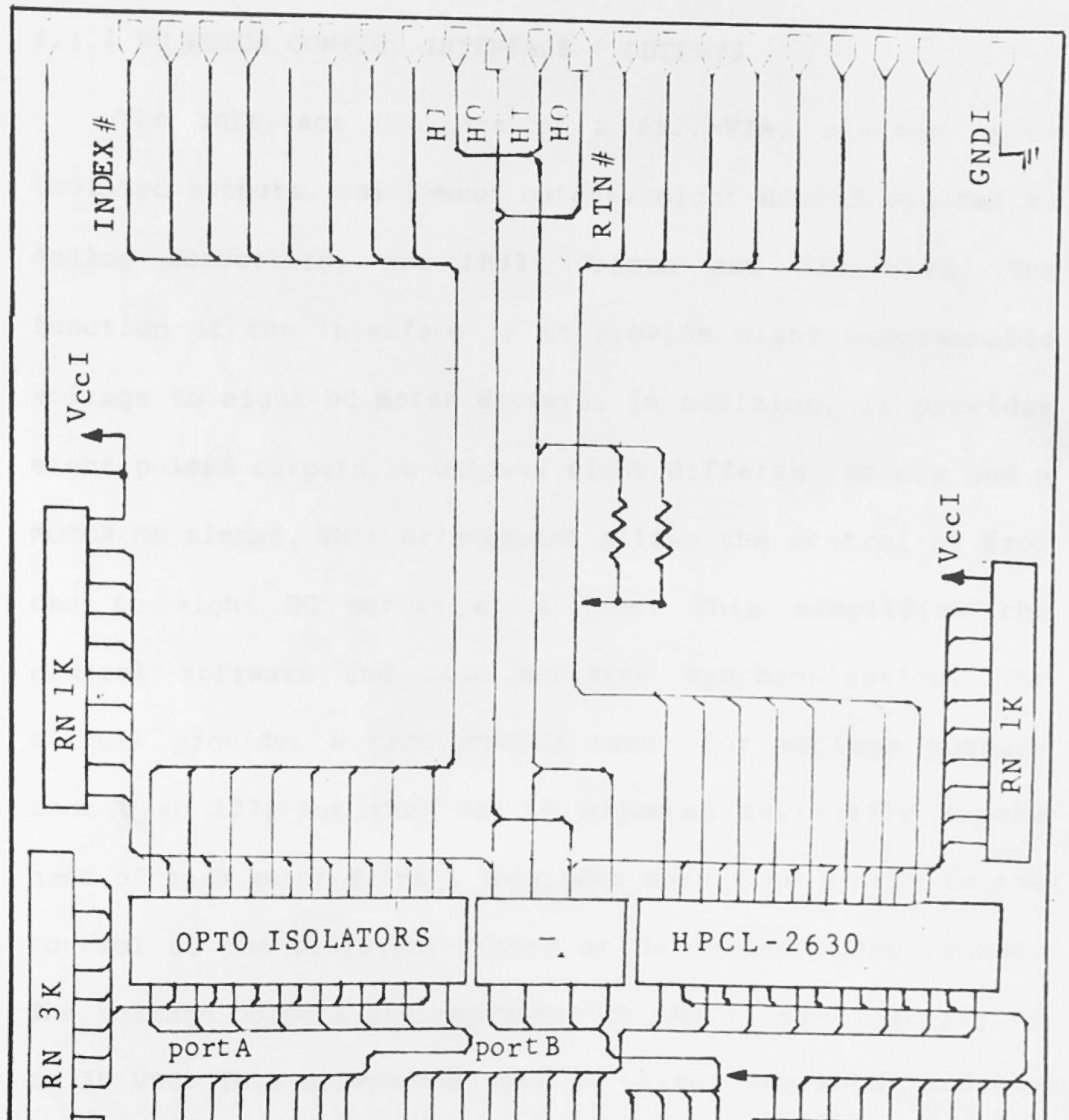


Figure 8 : STEPPING MOTOR INTERFACE CIRCUIT (INPUT)

4.1.4 DC MOTOR CONTROL INTERFACE (OUTPUTS)

The interface consists of a 6522-VIA, sixteen opto-isolated outputs, one 1-shot output, eight ADD558 Digital to Analog converters, two LM324 OpAmps and discretes. The function of the interface is to provide eight programmable voltage to eight DC motor drivers. In addition, it provides eight pulsed outputs to outputs eight different motors and a MOTOR ON signal. This arrangement allows the control of from one to eight DC motors at a time. This simplifies the control software and also achieves synchronization. The circuit provides a programmable range for voltage outputs from 0 to 127, but they can be adjusted invidually to the need of each motor driver. This adds more flexibility to the control of the different motors at different speed ranges. The voltage outputs are dependent on the external supply up to 30 VDC. This allows the user to select the motor and the power supply which is required.

Figure 9 shows the detail of the circuit. For programming, please see Appendix A.

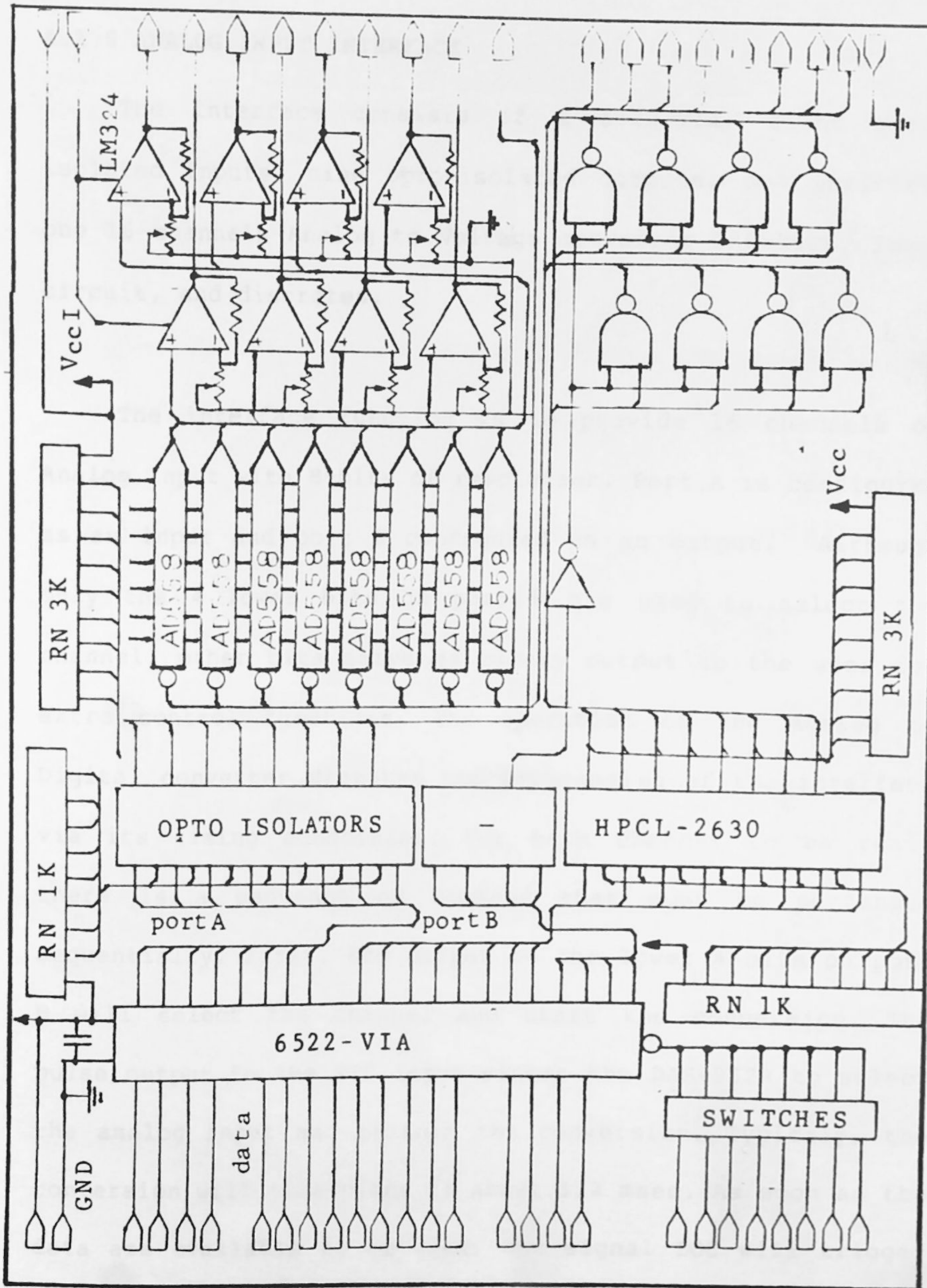


Figure 9 : DC MOTOR CONTROL INTERFACE (OUTPUTS)

4.1.5 ANALOG INPUT INTERFACE

The interface consists of a 6522-VIA, eight opto-isolated inputs, nine opto-isolated outputs, one inverter, one 16 channels Analog to Voltage converter DAS-952R, logic circuit, and discretes.

The interface function is to provide 16 channels of Analog input with 8-bits of resolution. Port A is configured as an input and port B configured as an output. Although only the 4 lower bits on port B are used to select the channel, other bits serve as binary output to the user for extra control functions. The operation of the Analog to Digital converter dictates the programming of the interface via its timing constraint. For each channel to be read, there is a sequence of command that must be performed sequentially. First, the output to the lower 4 bits on port B will select the channel and start the conversion. The pulse output to the STC input causes the DAS-952R to select the analog input and perform the conversion. Typicaly, the conversion will take place in about 1.2 msec. As soon as the data are available to be read, the signal EOC will trigger the 1-shot to create an output enable signal to the

DAS-952R. This signal also latches the output data onto port A. The data is now ready to be read from the computer. With a conversion rate of the DAS-952R, the computer can perform up to 10 conversions per second.

See Figure 10 for the detail of the circuit. For programming detail, please see Appendix A.

Figure 11 shows the timing requirement of the DAS-952R

4.2 DRIVER MODULES

4.2.1 STEPPER DRIVER

There are two different types of stepping motors which require different drives. There are also several drive methods such as full-wave, half-wave, etc. However, the efficiency of each drive is also dependent on the motor selection. The basis of this modular I/O design is to provide adjustability to the circuit to help the user establish some design goal.

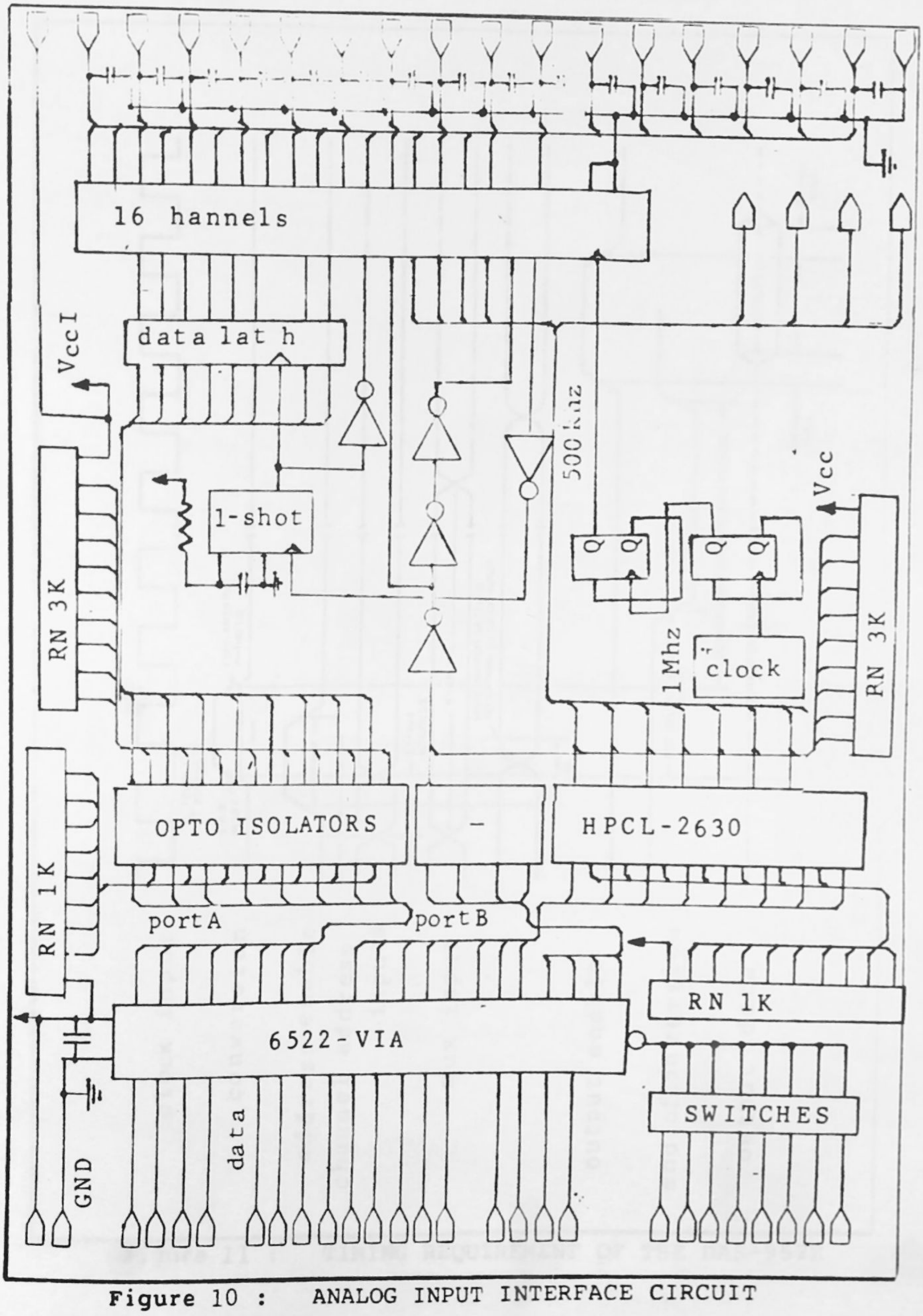


Figure 10 : ANALOG INPUT INTERFACE CIRCUIT

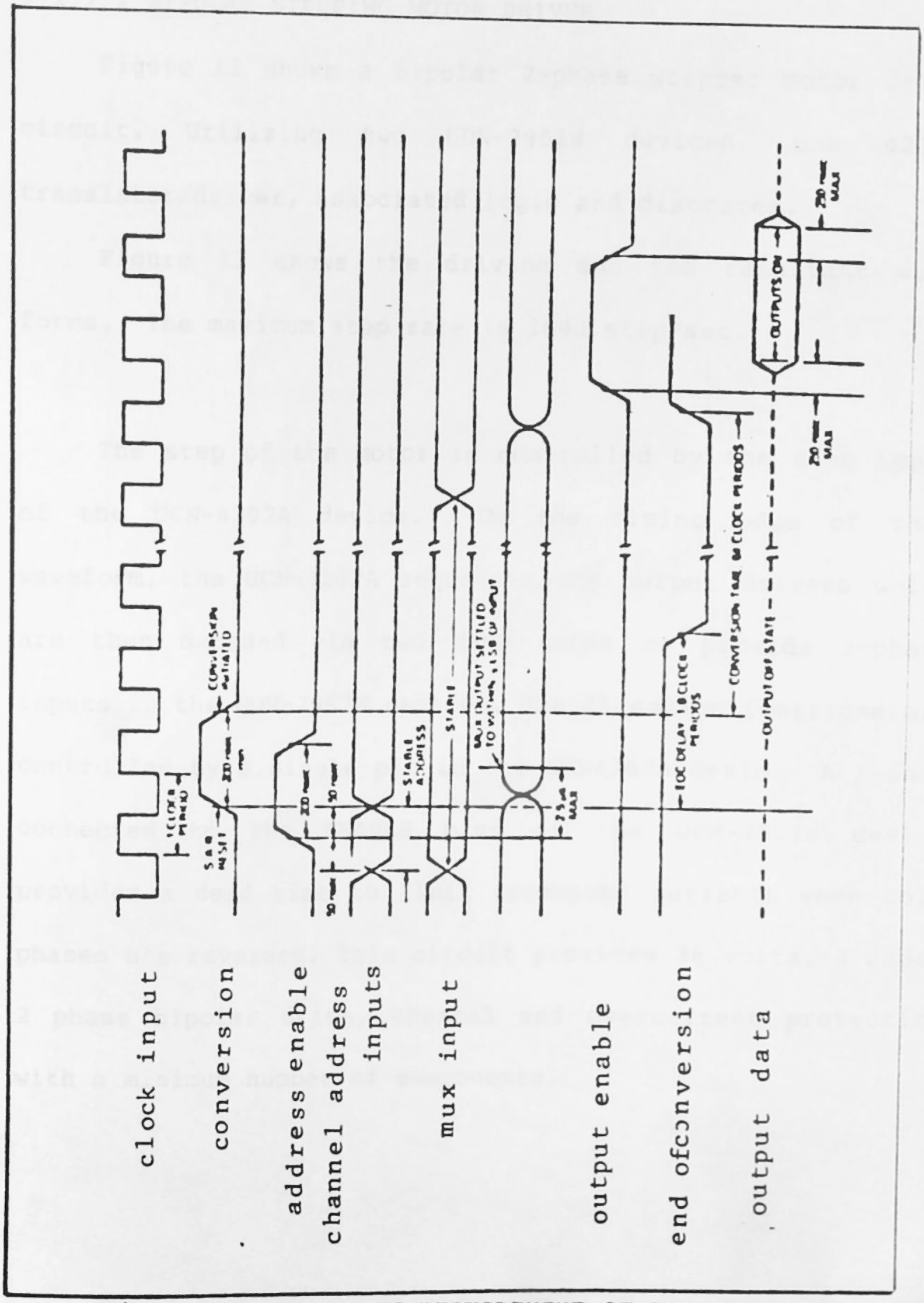


Figure 11 : TIMING REQUIREMENT OF THE DAS-952R

4.2.1.1 BIPOLAR STEPPING MOTOR DRIVER

Figure 12 shows a bipolar 2-phase stepper motor drive circuit. Utilizing two UDN-2952W devices, one 4202A translator/driver, associated logic and discretes.

Figure 13 shows the driving and the resultant wave forms. The maximum step rate is 1000 step/sec.

The step of the motor is controlled by the step input of the UCN-4202A device. On the rising edge of this waveform, the UCN-4202A sequences its output drivers which are then decoded via two NAND gates to provide 2-phase inputs to the UDN-2952W devices. The direction functions are controlled by a single pin in the UCN4202A device. A 1-shot connected to the ENABLE pins of the UDN-2952W device provides a dead time to limit crossover currents when coil phases are reversed. This circuit provides 36 volts, 2 amps, 2 phase bipolar drive, thermal and overcurrent protection with a minimum number of components.

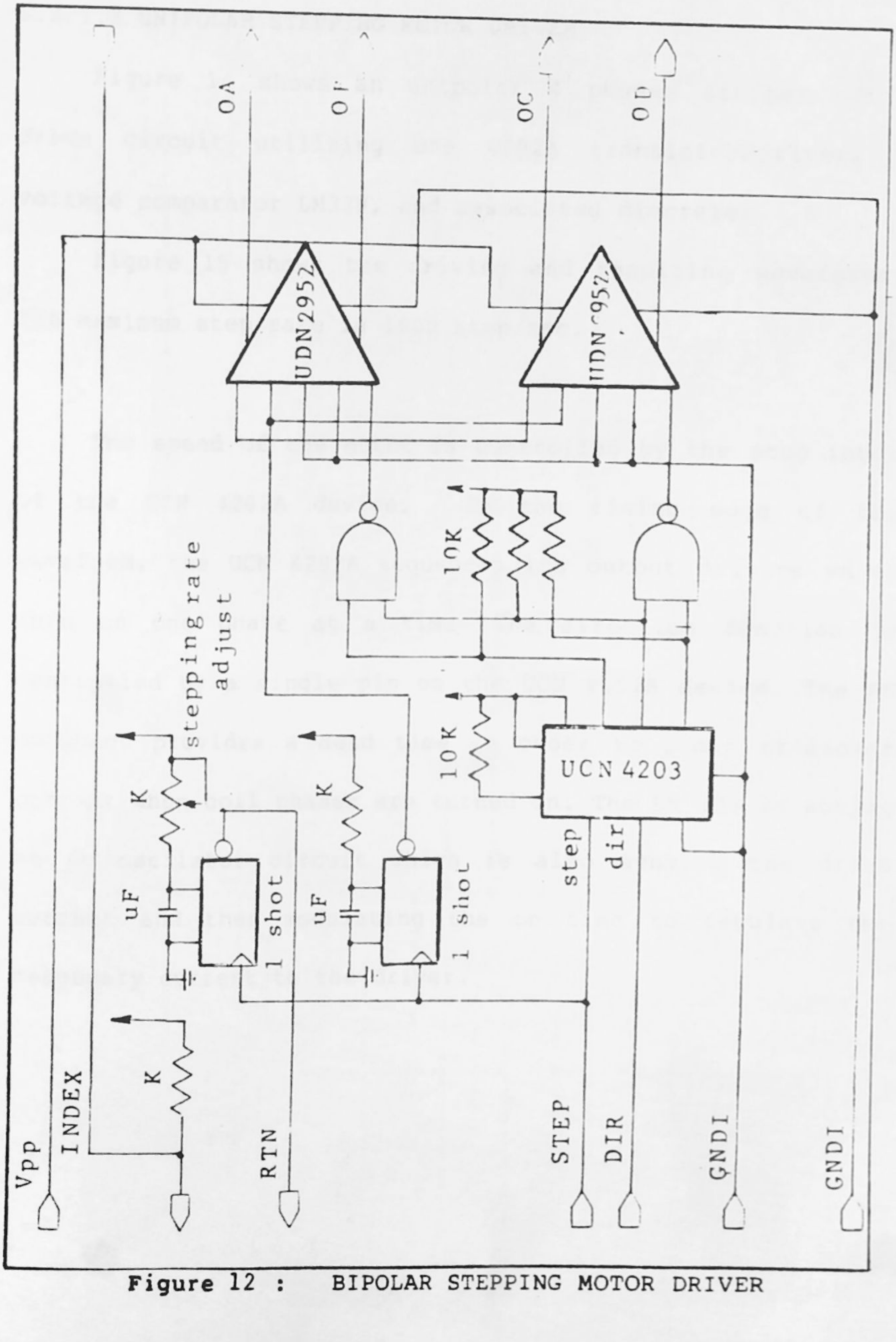


Figure 12 : BIPOLAR STEPPING MOTOR DRIVER

4.2.1.2 UNIPOLAR STEPPING MOTOR DRIVER

Figure 14 shows an unipolar 4 phases stepper motor drive circuit utilizing one 4202A translator/driver, a voltage comparator LM339, and associated discretes.

Figure 15 shows the driving and resulting waveforms. The maximum step rate is 1000 step/sec.

The speed of the motor is controlled by the step input of the UCN 4202A device. On the rising edge of the waveform, the UCN 4202A sequences its output drivers which turn on one phase at a time. The direction function is controlled by a single pin on the UCN 4202A device. The RC constant provides a dead time in order to limit crossover current when coil phases are turned on. The LM 339 is acting as an oscilator circuit which is also sensing the drive current and then modulating the on time to regulate the necessary current to the driver.

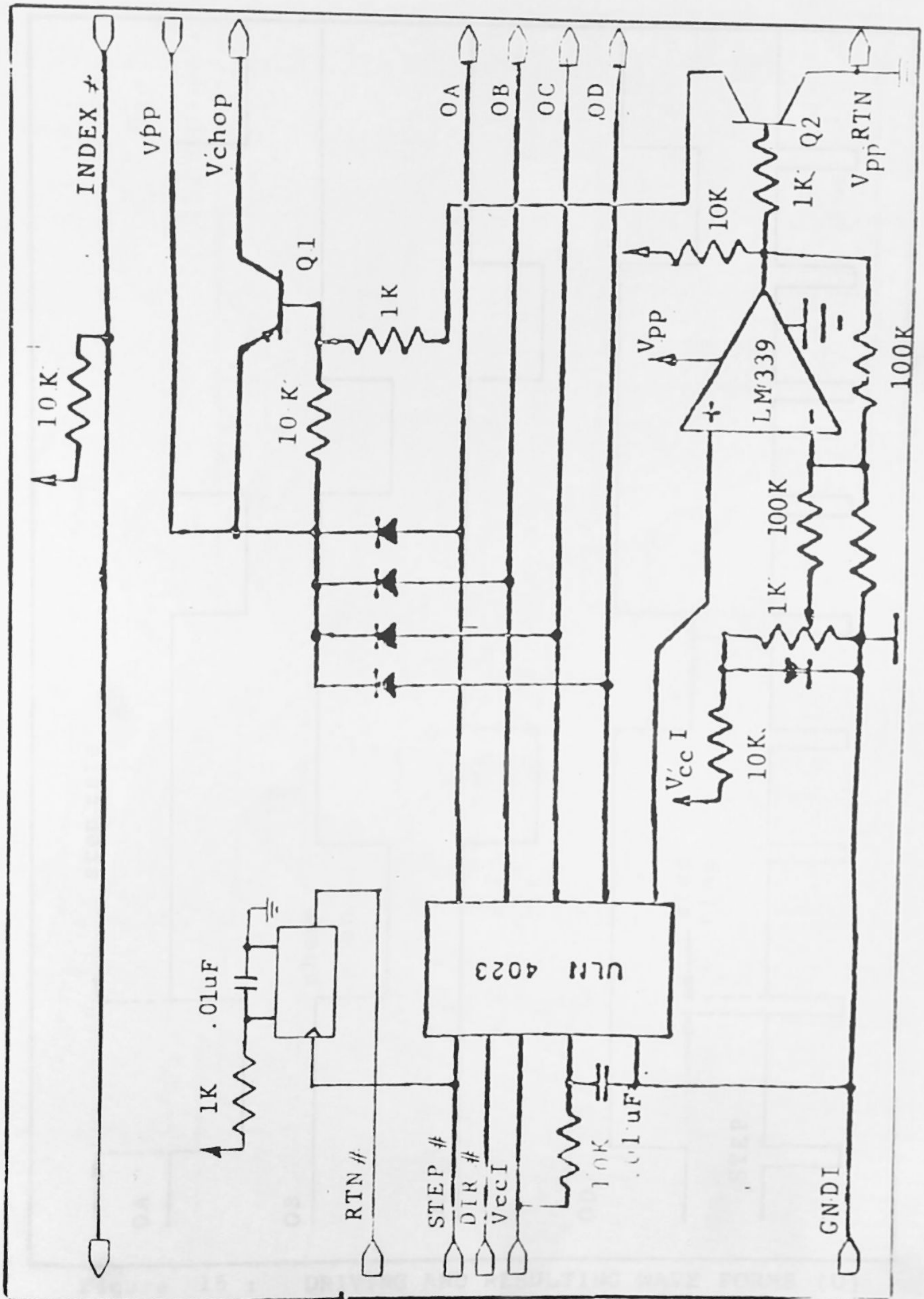


Figure 14 : UNIPOLAR STEPPER MOTOR DRIVER CIRCUIT

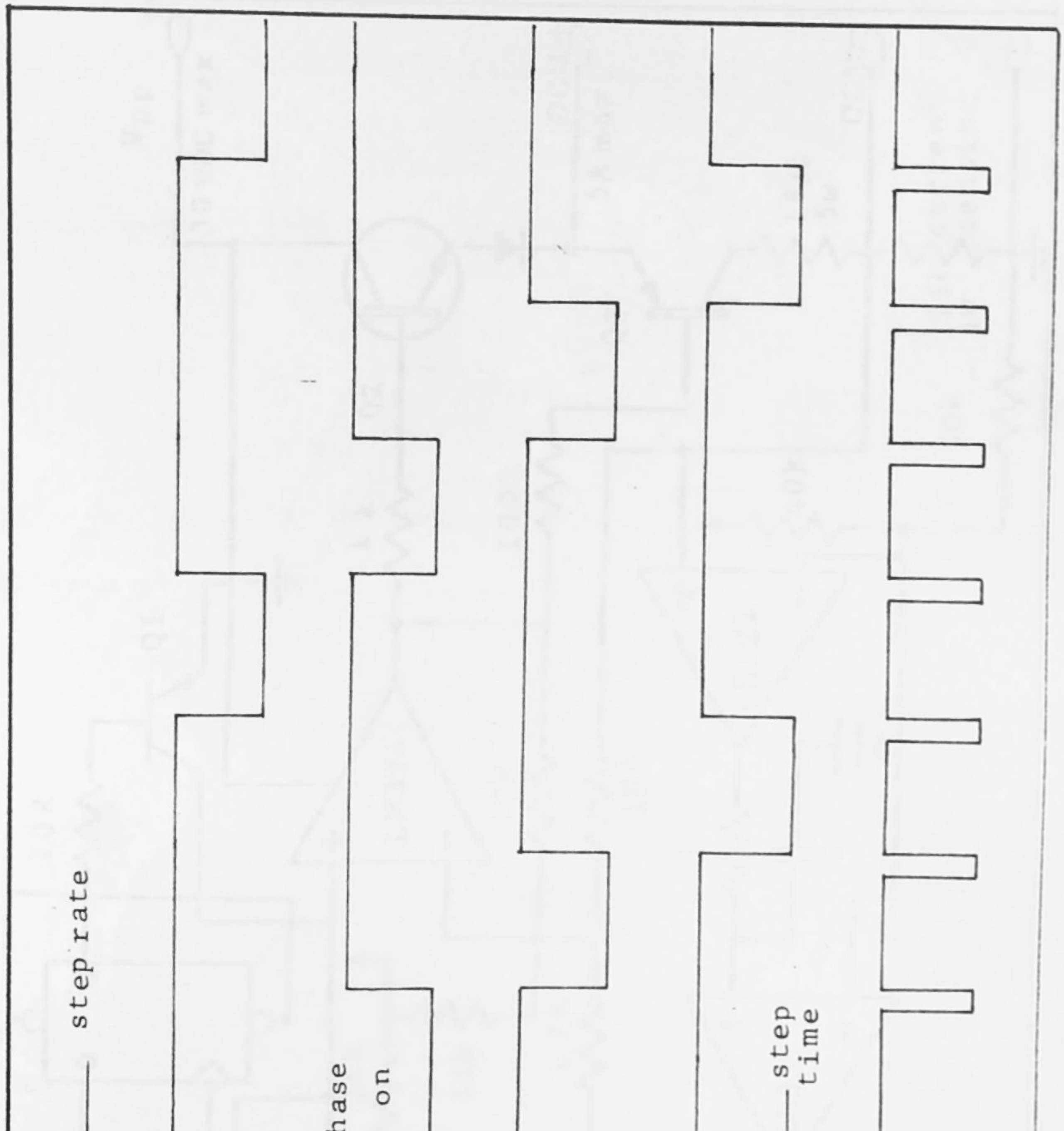


Figure 15 : DRIVING AND RESULTING WAVE FORMS (U)

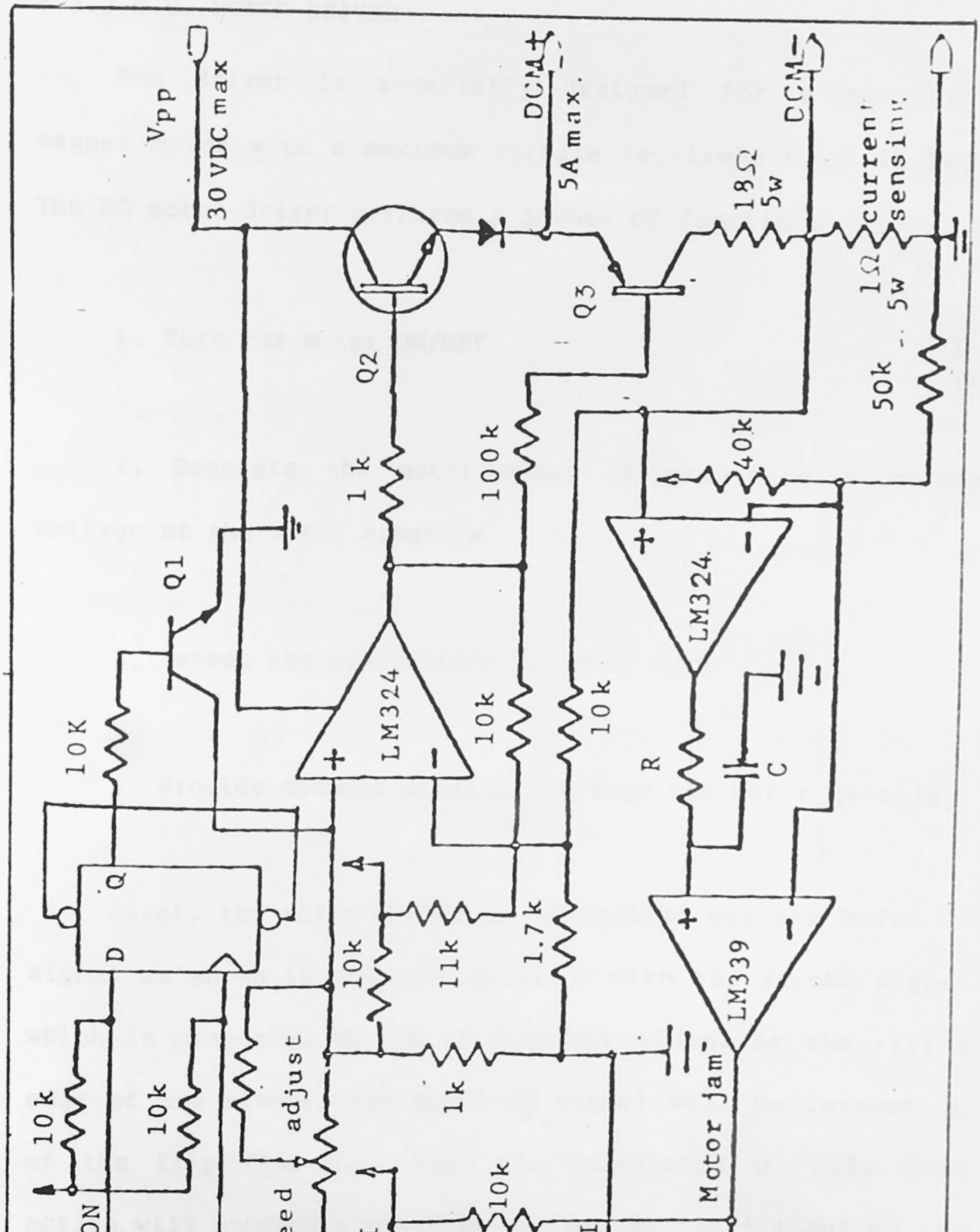


Figure 16 : DC MOTOR DRIVER

4.2.2 D.C. MOTOR DRIVER

The driver is especially designed for a permanent magnet motor with a maximum voltage requirement of 30 VDC. The DC motor driver performs a number of functions :

1. Turn the motor ON/OFF

2. Regulate the motor speed by providing a steady voltage at the motor armature

3. Detect the overcurrent or motor lock

4. Provide dynamic breaking to stop the motor quickly

First, the motor ON/OFF is controlled via the MOTOR ON signal as shown in the configuration with the strobe signal which is connected to one of 8 select lines. At the rising edge of the strobe, the MOTOR ON signal will be latched, Q of the flip flop will turn the transistor Q1 off. This action will produce a positive voltage at the + input of the op-amp. The op-amp in turn turns the transistor Q2 on. Thus current is allowed to flow to the motor. The voltage at the

+ input of the op-amp is always higher than the voltage at the - input in ON condition. If the motor is being turned OFF, the transistor Q1 will hold the + input to the op-amp below the - input to stop the current to flow into the motor.

Second, the motor speed is controlled by a programmed voltage source to the Vspeed input. The higher the input voltage, the higher the motor voltage. Since the motor speed is essentially directly proportional to this voltage, the increasing or decreasing of the Vspeed voltage, thus increases or decreases the motor speed. The speed is also regulated against torque variations by sensing the current in the armature. This current is directly proportional to the load.

Third, in the event that the load is increasingly heavy for the motor, the current sensing resistor will produce a voltage which is larger than the preset voltage. If this voltage is maintained larger than the set point for more than the preset time (RC contants) the motor is said to be jammed. This will produce the motorjam signal to the processor to stop the motor to prevent burn out.

Fourth, the motor can stop quickly by turning the transistor Q2 on. This action will allow the back emf voltage to be by passed to the DCM-terminal. This module is especially designed to be used with the DC motor interface module. However, it can be used in manual operation. The potentiometer RP1 provides the calibration of the motor speed versus Vspeed voltage.

Figure 16 shows the detail of the circuit. The device interface and the application are provided in Appendix B.

4.2.3 ANALOG CONDITIONING

The circuit is intended to provide scaling to an input voltage at a larger range than the reference voltage to the Analog to Digital conversion interface. In addition, it provides noise reduction capability to the system. The input voltage ranging from 0- to 30 VDC can be scaled down below the 5 DVC range with the potentiometer RP1. Since 5 VDC is the maximum voltage to the Analog to Digital interface, the calibration is often needed to set the maximum input voltage to get the full range by adjusting RP1 to get the scale factor.

For example, an input voltage from 0 to 30 VDC will be scaled to 0 to 5 VDC with scale factor 0.167. There is often an error of 5% introduced here. The user should be aware of this fact if precision is a concern.

Figure 17 shows the detail of the circuit. The interface detail is in Appendix B.

4.2.4 SPEED SENSING AND FREQUENCY TO VOLTAGE CONVERTER

The circuit in this module provides a means to sense the speed of a motor with a large frequency range. The input to the circuit could be an output from a phototransistor or a hall effect sensor. It may have a sine wave with a frequency which is proportional to the motor speed. The circuit has two main parts. The first is the speed sensing which is involved in detecting the peaks of the waveform and then establishing the threshold dynamically to detect the frequency and reject the high frequency noises. The second portion is the frequency to voltage conversion. The circuit is based on the LM 331 Frequency to Voltage conversion. The adjusting RP1 will set up maximum frequency to 5 VDC output. The proper scaling from the frequency to voltage can be done

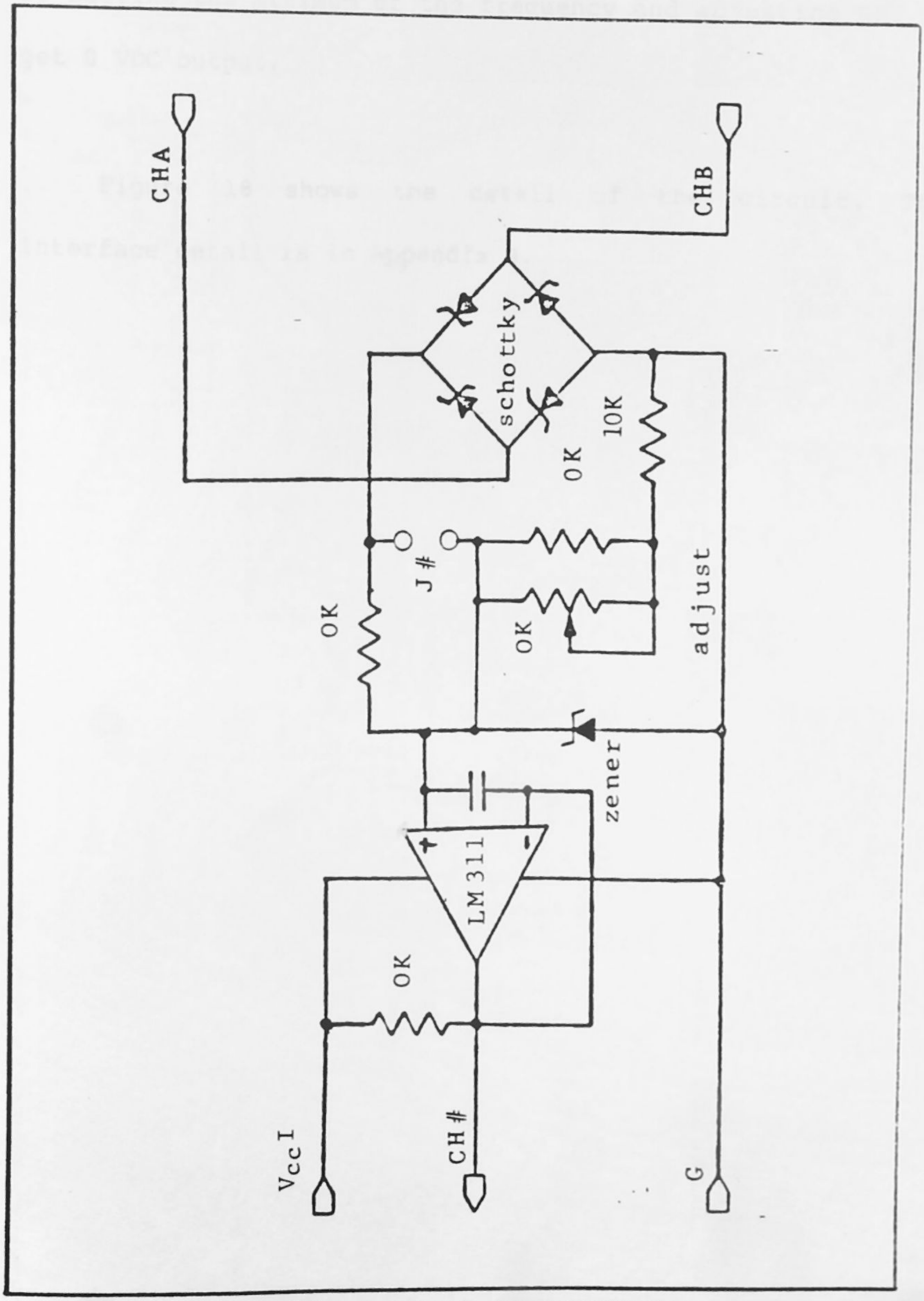


Figure 17 : ANALOG CONDITIONING

by setting the minimum of the frequency and adjusting RP2 to get 0 VDC output.

Figure 18 shows the detail of the circuit. The interface detail is in Appendix B.

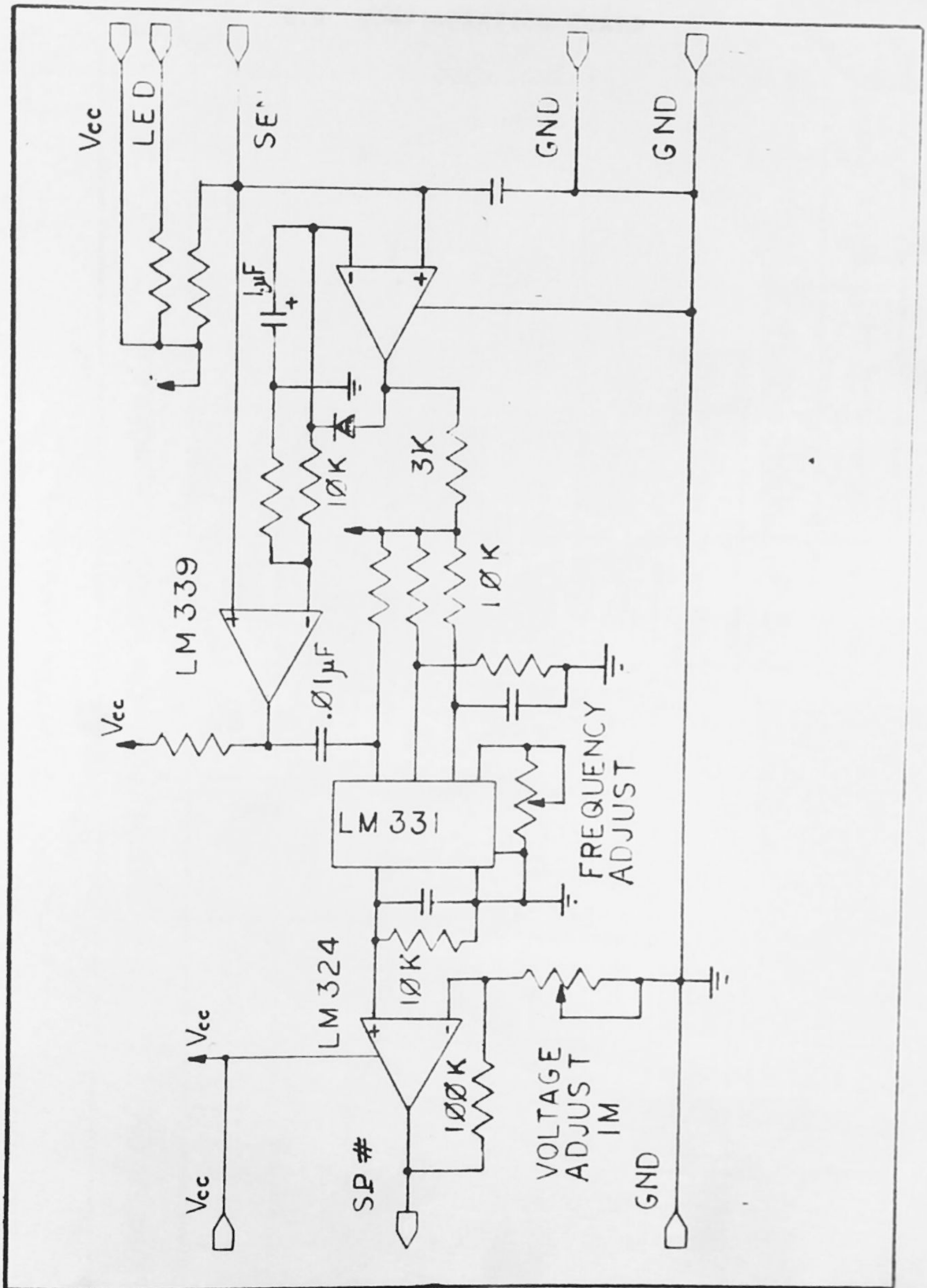


Figure 18 : SPEED SENSING & F/V CONVERTER

5.0 CONFIGURATION CHART

CONFIGURATION CHART.											
JUMPER ON				SWITCH ON INTERFACE MODULE							
J1	J2	J3	J4	S1	S2	S3	S4	S5	S6	S7	S8
				980x	982x	984x	986x	988x	98Ax	98Cx	98Ex
				990x	992x	994x	996x	998x	99Ax	99Cx	99Ex
				9A0x	9A2x	9A4x	9A6x	9A8x	9AAx	9ACx	9AEx
				9B0x	9B2x	9B4x	9B6x	9B8x	9Bax	9BCx	9BEx
				9C0x	9C2x	9C4x	9C6x	9C8x	9cAx	9CCx	9CEx
				9D0x	9D2x	9D4x	9D6x	9D8x	9DAx	9DCx	9dEx
				9E0x	9E2x	9E4x	9E6x	9E8x	9EAx	9ECx	9EEx
				9F0x	9F2x	9F4x	9F6x	9F8x	9FAx	9FCx	9FEx

Figure 19: CONFIGURATION CHART

6.0 CONCLUSION

The modular design has greatly simplified the design of the data acquisition process control system by reducing the hardware complexity and by providing the inherently flexible software implementation. The modular design permits several distinct process functions, each with distinct processing time requirements into one control unit thus allowing a broad range of application and adaptability.

The modular approach a process control system can be realized from a low cost personal computer. It is obvious that the approach will have certain value to industry as well as in the laboratory. The interface circuit design as an example of the approach is seen to have faced some limitation in terms of complexity and lack of invidualiity. However, the depth of these limitations is unpredictable. The drawback for these driver modules is the lack of generality. However, even with special hardware and dedicated equipment, such generality may not even exist.

As far as the implementation is concerned, the personal computer approach brings the convenience to the user particular with the popularity of the personal computer. The utility of the personal computer makes a perfect tool that is user friendly and easy to access. An abundance of control software and graphic capability will keep the personal computer to user interface at the touch of a button, a touch screen, a mouse or a joystick. These facilities are not likely to be as so easy with a dedicated process controller. The network software and linking capacity will allow the personal computer to be supervised from a mini or a main frame. It can also be able to share the resources, the data and the status from one to another thus making distributed control one step easier.

APPENDIX A

APPENDIX A

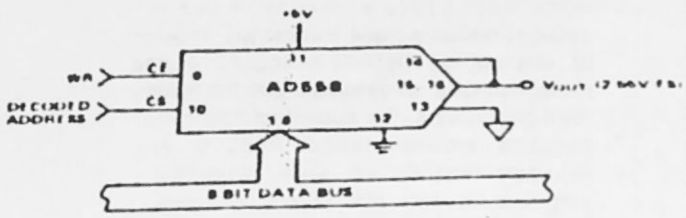
SELECTED COMPONENT SPECIFICATIONS

ANALOG DEVICES

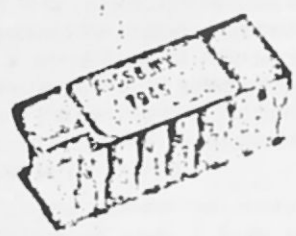
DACPORT™ Low Cost Complete μP-Compatible 8-Bit DAC

FEATURES

Complete 8-Bit DAC
Voltage Output – 2 Calibrated Ranges
Internal Precision Band-Gap Reference
Single-Supply Operation: +5V to +15V
Full Microprocessor Interface
Fast: 1μs Voltage Settling to ±1/2LSB
Low Power: 75mW
No User Trims
Guaranteed Monotonic Over Temperature
All Errors Specified T_{min} to T_{max}
Small 16-Pin DIP Package
Single Laser-Wafer-Trimmed Chip for Hybrids
Low Cost: $7.50 (100+, AD558JD)



AD558 SINGLE SUPPLY "DACPORT"



PRODUCT DESCRIPTION

The AD558 DACPORT is a complete voltage-output 8-bit digital-to-analog converter, including output amplifier, full microprocessor interface and precision voltage reference on a single monolithic chip. No external components or trims are required to interface, with full accuracy, an 8-bit data bus to an analog system.

The performance and versatility of the DACPORT is a result of several recently-developed monolithic bipolar technologies. The complete microprocessor interface and control logic is implemented with integrated injection logic (I^2L), an extremely dense and low-power logic structure that is process-compatible with linear bipolar fabrication. The internal precision voltage reference is the patented low-voltage band-gap circuit* which permits full-accuracy performance on a single +5V to +15V power supply. Thin-film silicon-chromium resistors provide the stability required for guaranteed monotonic operation over the entire operating temperature range (all grades), while recent advances in laser-wafer-trimming of these thin-film resistors permit absolute calibration at the factory to within ±1LSB; thus no user-trims for gain or offset are required. A new circuit design provides voltage settling to ±1/2LSB for a full-scale step in 800ns.

The AD558 is available in four performance grades. The AD558J and K are specified for use over the 0 to +70°C temperature range, while the AD558S and T grades are specified for –55°C to +125°C operation. The hermetically-sealed ceramic package is standard. Processing to MIL-STD-883, Class B is optional on S and T grades.

Figure A-1: ANALOG DEVICE : AD558

DATEL INTERSIL Data Acquisition System DAS-952R

FEATURES

- **16 Single Ended Channels**
- **8 Bits Resolution**
- **Monolithic CMOS Construction**
- **Three-State Outputs**
- **Ratiometric Operation**
- **Low Cost**

GENERAL DESCRIPTION

The DAS-952R is a single-chip 16 channel, 8 bit data acquisition system. Monolithic CMOS technology allows a 16 channel multiplexer, 8 bit successive approximation A/D converter, and microprocessor-compatible control logic to be fabricated on a single chip and contained in a compact Dual-In-Line package.

The design of this system emphasizes high accuracy, excellent repeatability, low power consumption, and a minimum of adjustments (no full scale or zero adjustment required). Latched and decoded address inputs and latched TTL three-state outputs allow easy interfacing to microprocessors.

The input multiplexer allows random access to any one of 16 single ended analog input channels and provides necessary logic for additional channel expansion. Connection of the multiplexer output to the converter input is by external pin connection, thus permitting easy signal conditioning such as amplification, linearization, or the use of a sample and hold.

The 8 bit A/D converter uses a 256R ladder network, successive approximation register, and a chopper-stabilized comparator to implement the successive approximation conversion technique with a switching tree. Use of 256R ladder network ensures monotonicity while the chopper-stabilizer comparator makes the converter highly resistant to thermal effects and long term drift. In ratiometric conversion, the converter expresses the analog value being measured as a percentage of reference input. Full scale range may be selected within limits, to adjust the sensitivity of the converter to the desired application or to refer the output to a secondary standard.

Accuracy, speed, flexibility, excellent performance over a wide temperature range (−25°C to +85°C) and low cost make the DAS-952R an easy and practical answer to many data acquisition needs.

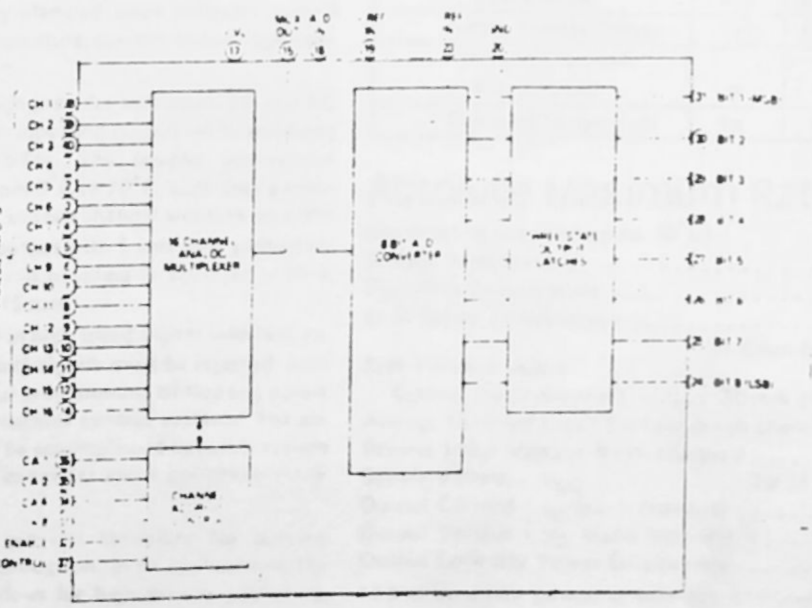


Figure A-2: DATA INTERSIL : DAS-952 R

HEWLETT PACKARD

DUAL TTL COMPATIBLE OPTOCOUPLER

HCPL-2630

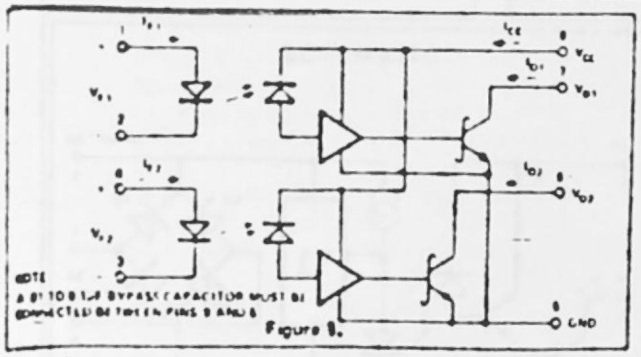


Figure 1.

Features

- HIGH DENSITY PACKAGING
- LSTTL/TTL COMPATIBLE: 5V SUPPLY
- ULTRA HIGH SPEED
- LOW INPUT CURRENT REQUIRED
- HIGH COMMON MODE REJECTION
- GUARANTEED PERFORMANCE OVER TEMPERATURE
- RECOGNIZED UNDER THE COMPONENT PROGRAM OF UNDERWRITERS LABORATORIES, INC. (FILE NO. E55361)
- DIELECTRIC WITHSTAND TESTED AT 2500 Vac FOR A WORKING VOLTAGE OF 220 Vac

Description/Applications

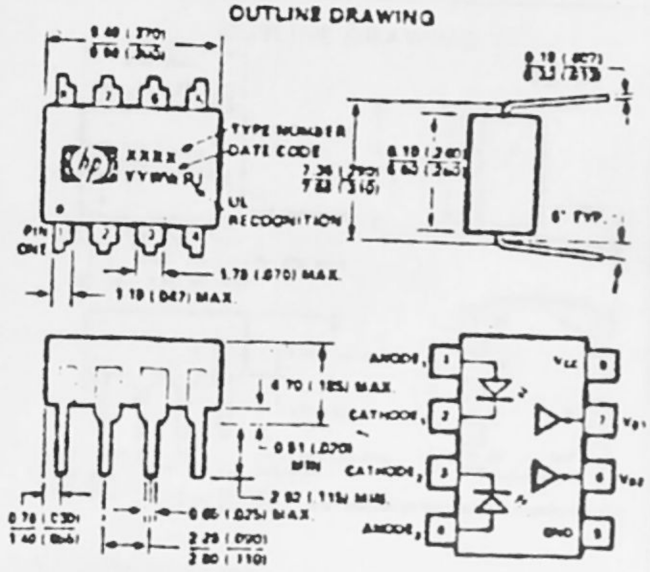
The HCPL-2630 consists of a pair of inverting optically coupled gates each with a GaAsP photon emitting diode and a unique integrated detector. The photons are collected in the detector by a photodiode and then amplified by a high gain linear amplifier that drives a Schottky clamped open collector output transistor. Each circuit is temperature, current and voltage compensated.

This unique dual coupler design provides maximum DC and AC circuit isolation between each input and output while achieving LSTTL/TTL circuit compability. The coupler operational parameters are guaranteed from 0°C to 70°C, such that a minimum input current of 5 mA in each channel will sink an eight gate fan-out (13 mA) at the output with 5 volt V_{CC} applied to the detector. This isolation and coupling is achieved with a typical propagation delay of 45 nsec.

The HCPL-2630 can be used in high speed digital interface applications where common mode signals must be rejected such as for a line receiver and digital programming of floating power supplies, motors, and other machine control systems. The elimination of ground loops can be accomplished between system interfaces such as between a computer and a peripheral memory, printer, controller, etc.

The open collector output provides capability for bussing, strobing and "WIRED-OR" connection. In all applications, the dual channel configuration allows for high density packaging, increased convenience and more usable board space.

OUTLINE DRAWING



DIMENSIONS IN MILLIMETRES AND (INCHES).

Recommended Operating Conditions

	Sym.	Min.	Max.	Units
Input Current, Low Level Each Channel	I_{FL}	0	250	μA
Input Current, High Level Each Channel	I_{FH}	6.3*	15	mA
Supply Voltage, Output	V_{CC}	4.5	5.5	V
Fan Out (TTL Load) Each Channel	N		8	
Operating Temperature	T_A	0	70	°C

Absolute Maximum Ratings

(No derating required up to 70°C)

Storage Temperature .... -55°C to +125°C
Operating Temperature .... 0°C to +70°C
Lead Solder Temperature .... 260°C for 10s (1.6mm below seating plane)
Peak Forward Input Current (each channel) ..... 30mA (≤1 msec Duration)
Average Forward Input Current (each channel) 15mA
Reverse Input Voltage (each channel) 5V
Supply Voltage - V_{CC} .... 7V (1 Minute Maximum)
Output Current - I_O (each channel) .... 16 mA
Output Voltage - V_O (each channel) 7V
Output Collector Power Dissipation .... 60 mW

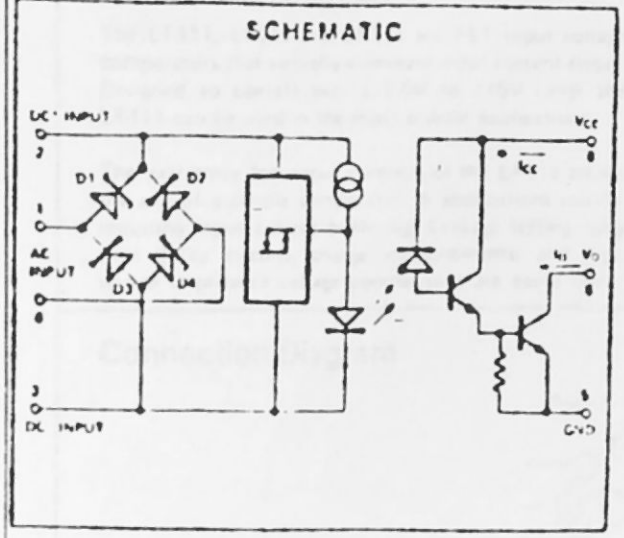
*6.3mA condition permits at least 20% CTR degradation guardband. Initial switching threshold is 5mA or less.

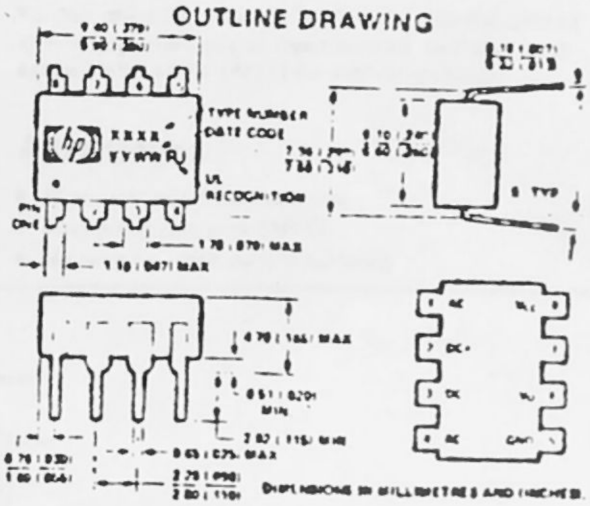
Figure A-3: HEWLETT PACKARD : HPCL-2630

HEWLETT PACKARD

AC/DC TO LOGIC INTERFACE OPTOCOUPLER

HCPL-3700



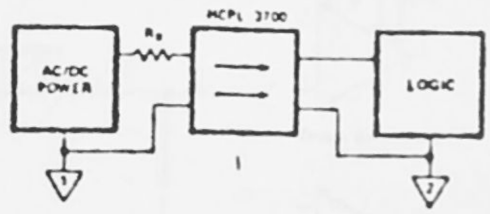


Features

- AC OR DC INPUT
- PROGRAMMABLE SENSE VOLTAGE
- HYSTERESIS
- LOGIC COMPATIBLE OUTPUT
- SMALL SIZE: STANDARD 8 PIN DIP
- THRESHOLDS GUARANTEED OVER TEMPERATURE
- THRESHOLDS INDEPENDENT OF LED DEGRADATION
- DIELECTRIC WITHSTAND TESTED AT 2500 Vac FOR A WORKING VOLTAGE OF 220 Vac
- RECOGNIZED UNDER THE COMPONENT PROGRAM OF UNDERWRITERS LABORATORIES, INC. (FILE NO. E55361)

Applications

- LIMIT SWITCH SENSING
- LOW VOLTAGE DETECTOR
- 5V—240V AC/DC VOLTAGE SENSING
- RELAY CONTACT MONITOR
- RELAY COIL VOLTAGE MONITOR
- CURRENT SENSING
- MICROPROCESSOR INTERFACING



Description

The HCPL-3700 is a voltage/current threshold detection optocoupler. This optocoupler uses an internal Light Emitting Diode (LED), a threshold sensing input buffer IC, and a high gain photon detector to provide an optocoupler which permits adjustable external threshold levels. The input buffer circuit has a nominal turn on threshold of 2.5 mA (I_{TH+}) and 3.8 volts (V_{TH+}). The addition of one or more external attenuation resistors permits the use of this device over a wide range of input voltages and currents. Threshold sensing prior to the LED and detector elements minimizes effects of different optical gain and LED variations over operating life (CTR degradation). Hysteresis is also provided in the buffer for extra noise immunity and switching stability.

The buffer circuit is designed with internal clamping diodes to protect the circuitry and LED from a wide range of over-voltage and over-current transients while the diode bridge enables easy use with ac voltage input.

The high gain output stage features an open collector output providing both TTL compatible saturation voltages and CMOS compatible breakdown voltages.

The HCPL-3700, by combining several unique functions in a single package, provides the user with an ideal component for industrial control computer input boards and other applications where a predetermined input threshold optocoupler level is desirable.

Figure A-4: HEWLETT PACKARD : HPCL-3700

National Semiconductor — Voltage Comparators

LF111/LF211/LF311 Voltage Comparators

General Description

The LF111, LF211 and LF311 are FET input voltage comparators that virtually eliminate input current errors. Designed to operate over a 5.0V to ±15V range the LF111 can be used in the most critical applications.

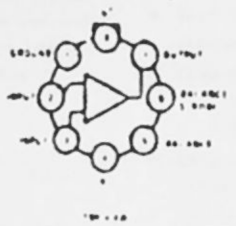
The extremely low input currents of the LF111 allows the use of a simple comparator in applications usually requiring input current buffering. Leakage testing, long time delay circuits, charge measurements, and high source impedance voltage comparisons are easily done. Further, the LF111 can be used in place of the LM111 eliminating errors due to input currents. See the "application hints" of the LM311 for application help.

Advantages

- Eliminates input current errors
- Interchangeable with LM111
- No need for input current buffering

Connection Diagram

Metal Can Package



Order Number LF111H, LF211H or LF311H
See NS Package H08C

Schematic Diagram and Auxiliary Circuits

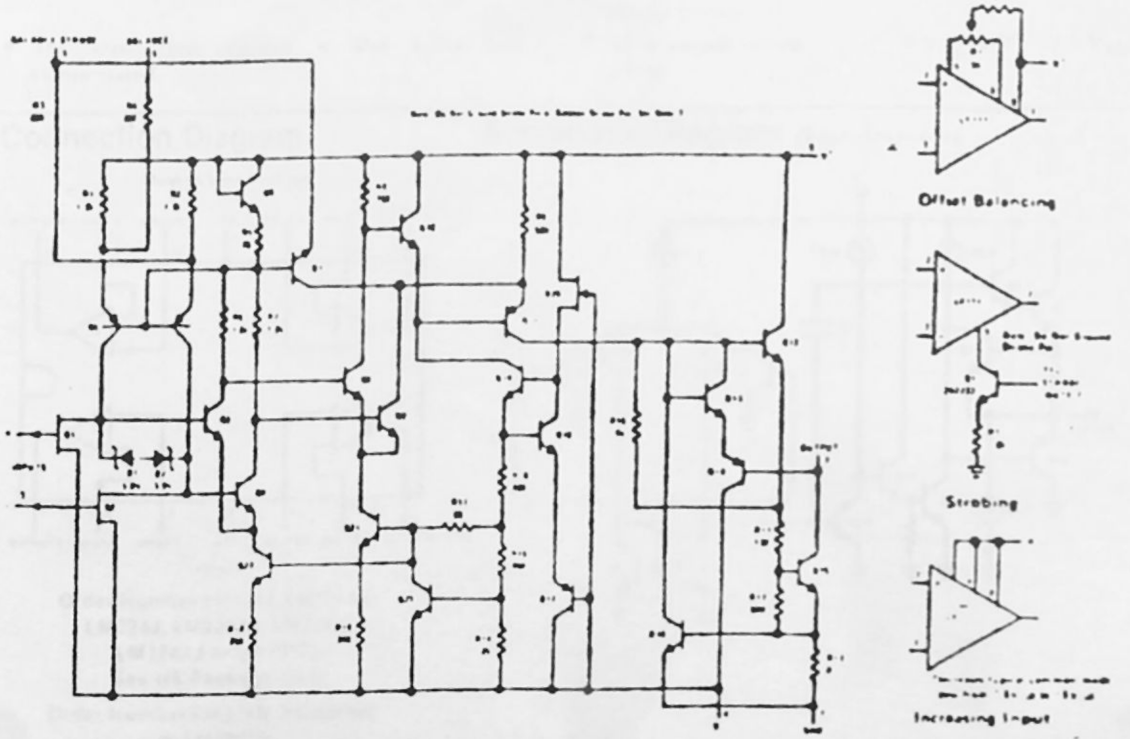


Figure A-5: NATIONAL SEMICONDUCTOR : LF311

National Semiconductor

Operational Amplifiers/Buffers

LM124/LM224/LM324, LM124A/LM224A/LM324A, LM2902 Low Power Quad Operational Amplifiers

General Description

The LM124 series consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, dc gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM124 series can be directly operated off of the standard +5 V_{DC} power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15 V_{DC} power supplies.

Unique Characteristics

- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage
- The unity gain cross frequency is temperature compensated
- The input bias current is also temperature compensated

Advantages

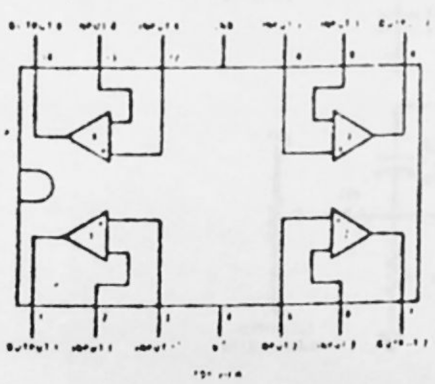
- Eliminates need for dual supplies
- Four internally compensated op amps in a single package
- Allows directly sensing near GND and V_{OUT} also goes to GND
- Compatible with all forms of logic
- Power drain suitable for battery operation

Features

- Internally frequency compensated for unity gain
- Large dc voltage gain 100 dB
- Wide bandwidth (unity gain) 1 MHz (temperature compensated)
- Wide power supply range
  - Single supply 3 V_{DC} to 30 V_{DC}
  - or dual supplies ±1.5 V_{DC} to ±15 V_{DC}
- Very low supply current drain (800 μA) — essentially independent of supply voltage (1 mW/op amp at +5 V_{DC})
- Low input biasing current 45 nA_{DC} (temperature compensated)
- Low input offset voltage 2 mV_{DC} and offset current 5 nA_{DC}
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing 0 V_{DC} to V^{+} − 1.5 V_{DC}

Connection Diagram

Dual-In-Line Package



Top View

Order Number LM124J, LM124AJ, LM224J, LM224AJ, LM324J, LM324AJ or LM2902J
See NS Package J14A

Order Number LM324N, LM324AN or LM2902N

Schematic Diagram (Each Amplifier)

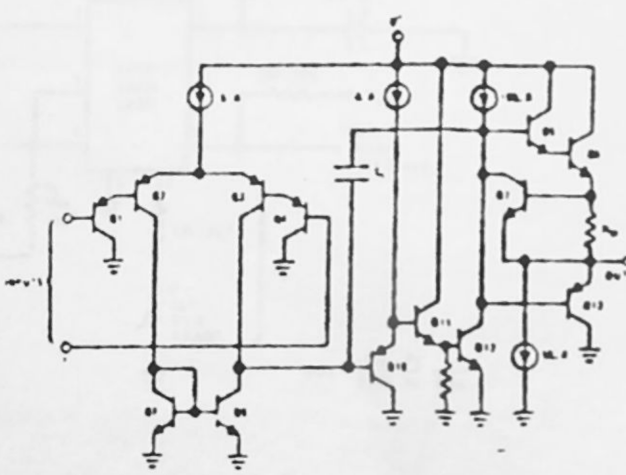


Figure A-6: NATIONAL SEMICONDUCTOR : LM324

National Semiconductor

A to D, D to A

LM131A/LM131, LM231A/LM231, LM331A/LM331 Precision Voltage-to-Frequency Converters

General Description

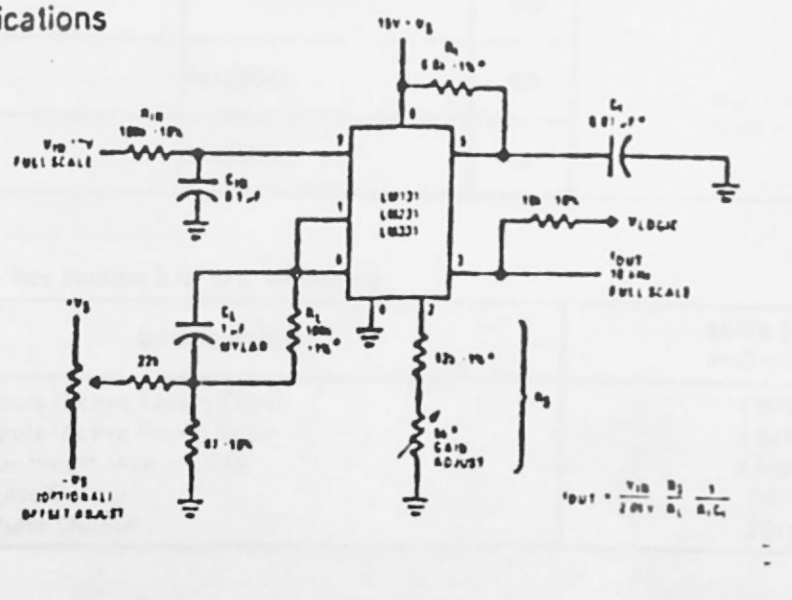
The LM131/LM231/LM331 family of voltage-to-frequency converters are ideally suited for use in simple low-cost circuits for analog-to-digital conversion, precision frequency-to-voltage conversion, long-term integration, linear frequency modulation or demodulation, and many other functions. The output when used as a voltage-to-frequency converter is a pulse train at a frequency precisely proportional to the applied input voltage. Thus, it provides all the inherent advantages of the voltage-to-frequency conversion techniques, and is easy to apply in all standard voltage-to-frequency converter applications. Further, the LM131A/LM231A/LM331A attains a new high level of accuracy versus temperature which could only be attained with expensive voltage-to-frequency modules. Additionally the LM131 is ideally suited for use in digital systems at low power supply voltages and can provide low-cost analog-to-digital conversion in microprocessor-controlled systems. And, the frequency from a battery powered voltage-to-frequency converter can be easily channeled through a simple photoisolator to provide isolation against high common mode levels.

The LM131/LM231/LM331 utilizes a new temperature-compensated band-gap reference circuit, to provide excellent accuracy over the full operating temperature range, at power supplies as low as 4.0V. The precision timer circuit has low bias currents without degrading the quick response necessary for 100 kHz voltage-to-frequency conversion. And the output is capable of driving 3 TTL loads, or a high voltage output up to 40V, yet is short-circuit-proof against V_{CC}.

Features

- Guaranteed linearity 0.01% max
- Improved performance in existing voltage-to-frequency conversion applications
- Split or single supply operation
- Operates on single 5V supply
- Pulse output compatible with all logic forms
- Excellent temperature stability, ±50 ppm/°C max
- Low power dissipation, 15 mW typical at 5V
- Wide dynamic range, 100 dB min at 10 kHz full scale frequency
- Wide range of full scale frequency, 1 Hz to 100 kHz
- Low cost

Typical Applications



*Use stable components with low temperature coefficients. See Typical Applications section.

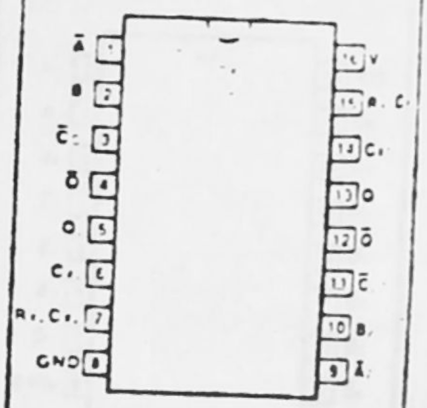
FIGURE 1. Simple Stand Alone Voltage-to-Frequency Converter with ±0.03% Typical Linearity (f = 10 Hz to 11 kHz)

Figure A-7: NATIONAL SEMICONDUCTOR : LM331

54/74123

DUAL RETRIGGERABLE RESETTABLE MULTIVIBRATOR

CONNECTION DIAGRAM
PINOUT A

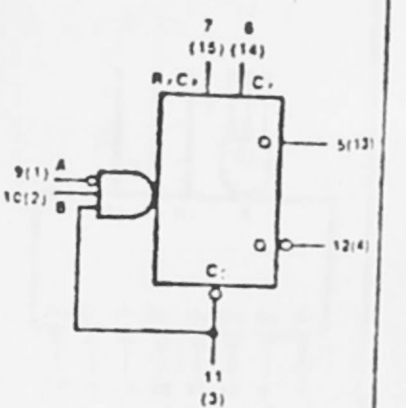


DESCRIPTION — Each half of the '123 features retriggerable capability, complementary dc level triggering and overriding Direct Clear. When a circuit is in the quasi-stable (delay) state, another trigger applied to the inputs (per the Truth Table) will cause the delay period to start again, without disturbing the outputs. By repeating this process, the output pulse period (Q HIGH, $\bar{Q}$ LOW) can be made as long as desired. Alternatively, a delay period can be terminated at any time by a LOW signal on $\bar{C}_D$, which also inhibits triggering. An internal connection from $\bar{C}_D$ to the input gate makes it possible to trigger the circuit by a positive-going signal on $\bar{C}_D$, as shown in the Truth Table. For timing capacitor values greater than 1000 pF, the output pulse width is defined as follows

$$t_w = 0.28\, R_X C_X \,(1.0 + 0.7/R_X)$$

Where t_w is in ns, R_X is in kΩ and C_X is in pF.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74123PC		9B
Ceramic DIP (D)	A	74123DC	54123DM	6B
Flatpak (F)	A	74123FC	54123FM	4L

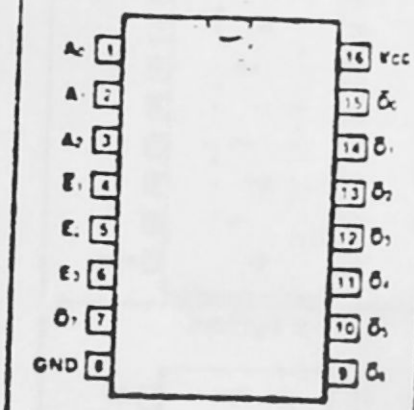
INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
$\bar{A}_1$, $\bar{A}_2$	Trigger Inputs (Active Falling Edge)	1.0/1.0
B_1, B_2	Trigger Inputs (Active Rising Edge)	1.0/1.0
$\bar{C}_{D1}$, $\bar{C}_{D2}$	Direct Clear Inputs (Active LOW)	2.0/2.0
Q_1, Q_2	Positive Pulse Output	20/10
$\bar{Q}_1$, $\bar{Q}_2$	Negative Pulse Output	20/10

Figure A-8: NATIONAL SEMICONDUCTOR : 74LS123

54S/74S138
54LS/74LS138
1-OF-8 DECODER/DEMULTIPLEXER

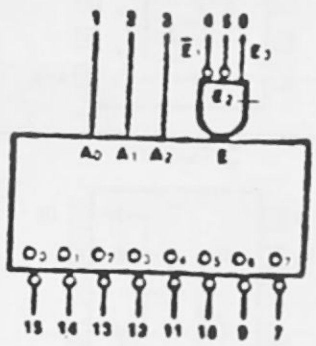
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '138 is a high speed 1-of-8 decoder/demultiplexer. This device is ideally suited for high speed bipolar memory chip select address decoding. The multiple input enables allow parallel expansion to a 1-of-24 decoder using just three '138 devices or to a 1-of-32 decoder using four '138 devices and one inverter. The '138 is fabricated with the Schottky barrier diode process for high speed.

- **SCHOTTKY PROCESS FOR HIGH SPEED**
- **DEMULTIPLEXING CAPABILITY**
- **MULTIPLE INPUT ENABLE FOR EASY EXPANSION**
- **ACTIVE LOW MUTUALLY EXCLUSIVE OUTPUTS**

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74S138PC, 74LS138PC		9B
Ceramic DIP (D)	A	74S138DC, 74LS138DC	54S138DM, 54LS138DM	6B
Flatpak (F)	A	74S138FC, 74LS138FC	54S138FM, 54LS138FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$A_0 - A_2$	Address Inputs	1.25/1.25	0.5/0.25
$\overline{E}_1$, $\overline{E}_2$	Enable Inputs (Active LOW)	1.25/1.25	0.5/0.25
E_3	Enable Input (Active HIGH)	1.25/1.25	0.5/0.25
$\overline{O}_0 - \overline{O}_7$	Outputs (Active LOW)	25/12.5	10/5.0 (2.5)

Figure A-9: NATIONAL SEMICONDUCTOR : 74LS138

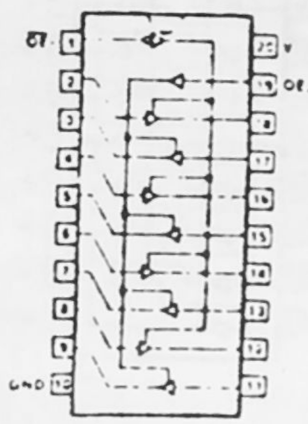
54S/74S240 • 54LS/74LS240
54S/74S241 • 54LS/74LS241
54LS/74LS244

OCTAL BUFFER/LINE DRIVER
(With 3-State Outputs)

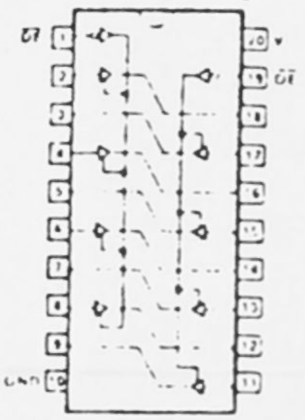
CONNECTION DIAGRAMS

PINOUT A

PINOUT B



PINOUT C



DESCRIPTION — The '240, '241 and '244 are octal buffers and line drivers designed to be employed as memory address drivers, clock drivers and bus oriented transmitters/receivers which provide improved PC board density.

- HYSTERESIS AT INPUTS TO IMPROVE NOISE MARGINS
- 3-STATE OUTPUTS DRIVE BUS LINES OR BUFFER MEMORY ADDRESS REGISTERS
- OUTPUTS SINK 24 mA (74LS) OR 40 mA (74S)
- 15 mA SOURCE CURRENT
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74S240PC, 74LS240PC		9Z
	B	74S241PC, 74LS241PC		
	C	74LS244PC		
Ceramic DIP (D)	A	74S240DC, 74LS240DC	54S240DM, 54LS240DM	4E
	B	74S241DC, 74LS241DC	54S241DM, 54LS241DM	
	C	74LS244DC	54LS244DM	
Flatpak (F)	A	74S240FC, 74LS240FC	54S240FM, 54LS240FM	4F
	B	74S241FC, 74LS241FC	54S241FM, 54LS241FM	
	C	74LS244FC	54LS244FM	

INPUT LOADING/FAN-OUT: See Section 9

PIN NAMES	DESCRIPTION	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$\overline{OE}_1$, $\overline{OE}_2$	3-State Output Enable (Active LOW)	1.25/1.25	0.5/0.25
OE_2	3-State Output Enable (Active HIGH)	1.25/1.25	0.5/0.25
	Inputs	1.25/0.25	0.5/0.125
	Outputs	75/40 (30)	75/15 (7.5)

Figure A-10: NATIONAL SEMICONDUCTOR : 74LS240

54LS/74LS245

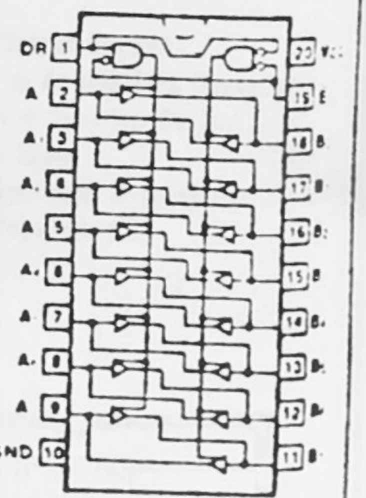
OCTAL BUS TRANSCEIVER

(With 3-State Outputs)

DESCRIPTION — The 'LS245 is an octal bus transmitter/receiver designed for 8-line asynchronous 2-way data communication between data busses. Direction input (DR) controls transmission of data from bus A to bus B or bus B to bus A depending upon its logic level. The Enable input ($\overline{E}$) can be used to isolate the busses.

- HYSTERESIS INPUTS TO IMPROVE NOISE IMMUNITY
- 2-WAY ASYNCHRONOUS DATA BUS COMMUNICATION
- INPUT DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	74LS245PC		9Z
Ceramic DIP (D)	A	74LS245DC	54LS245DM	4E
Flatpak (F)	A	74LS245FC	54LS245FM	4F

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74LS (U.L.) HIGH/LOW
Inputs	0.5/0.125
Outputs	75/15 (7.5)

TRUTH TABLE

INPUTS $\overline{E}$	INPUTS DR	OUTPUT
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	Isolation

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Figure A-11: NATIONAL SEMICONDUCTOR : 74LS245

UCN-4202A AND UCN-4203A STEPPER-MOTOR TRANSLATORS AND DRIVERS

a Penn Central unit

DESIGNED TO DRIVE permanent-magnet stepper motors with current ratings of up to 500 mA, these integrated circuits employ a full-step, double-pulse drive scheme that allows use of up to 90 percent of available motor torque. The two devices differ only in output-voltage ratings: Type UCN-4202A has a 20 V breakdown-voltage rating and a 15 V sustaining voltage rating; Type UCN-4203A has a 50 V breakdown-voltage rating and a 35 V sustaining voltage rating.

Both drivers are bipolar I^2L designs containing approximately 100 logic gates, TTL-compatible input/output circuitry, and 600 mA outputs with internal transient suppressors. The devices operate with a minimum of external components.

The four-phase stepper-motor load is controlled by step-logic functions. To step the load from one position to the next, STEP INPUT is pulled down to a logic low for at least 1 μs, then allowed to return to a logic high. The step logic is activated on the positive-going edge, which in turn activates one of the four current-sink outputs. DIRECTION CONTROL determines the sequence of states (A-B-C-D or A-D-C-B).

In the full-step mode, the MONOSTABLE RC timing pin is tied to V_{CC}, making states B and D stationary. A separate input pulse is required to move through each of the four output states.

In the double-step mode, states B and D are transition states with duration determined by MONOSTABLE RC timing. Improved motor torque is obtained at double the nominal motor step angle, and motor stability is improved for high step rates.

Higher current ratings, or bipolar operation, can be obtained by using Type UCN-4202A or UCN-4203A as a logic translator to drive integrated motor drivers (Sprague Type UDN-2949Z or UDN-2952B/W) or discrete high-power transistors.

FEATURES

- 600 mA Output Current
- Full-Step or Double-Step Operation
- Single-Input Direction Control
- Power-On Reset
- Internal Transient Suppression
- Schmitt Trigger Inputs

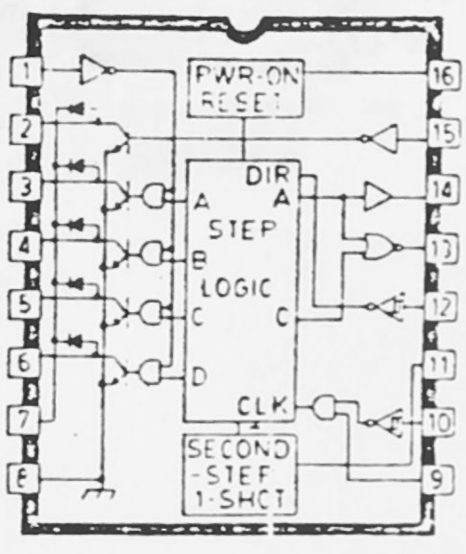


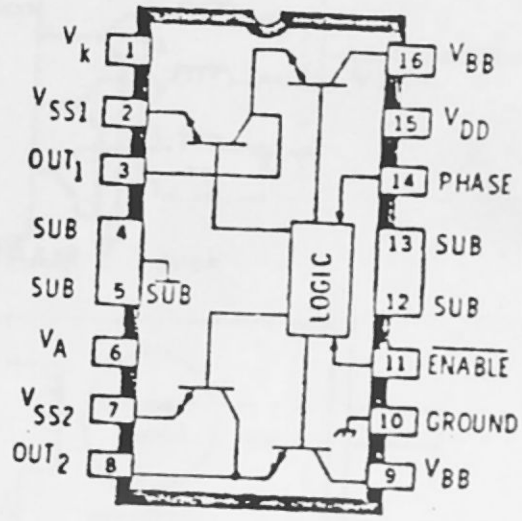
Figure A-13: SPRAGUE : UCN-4203A

UDN-2952B AND UDN-2952W FULL-BRIDGE MOTOR DRIVERS

a Penn Central unit

FEATURES

- High Output Current
- Adjustable Short-Circuit Protection
- Thermal Protection
- Internal Clamp Diodes
- TTL, DTL, PMOS, CMOS Compatible
- DIP or SIP Packaging



UDN-2952B

FULL-BRIDGE MOTOR-DRIVER integrated circuits, Types UDN-2952B and UDN-2952W combine low-level logic circuitry and Darlington output power drivers for bidirectional control of d-c motors or solenoids operating with continuous load currents of up to 2A and peak start-up currents as high as 3.5A.

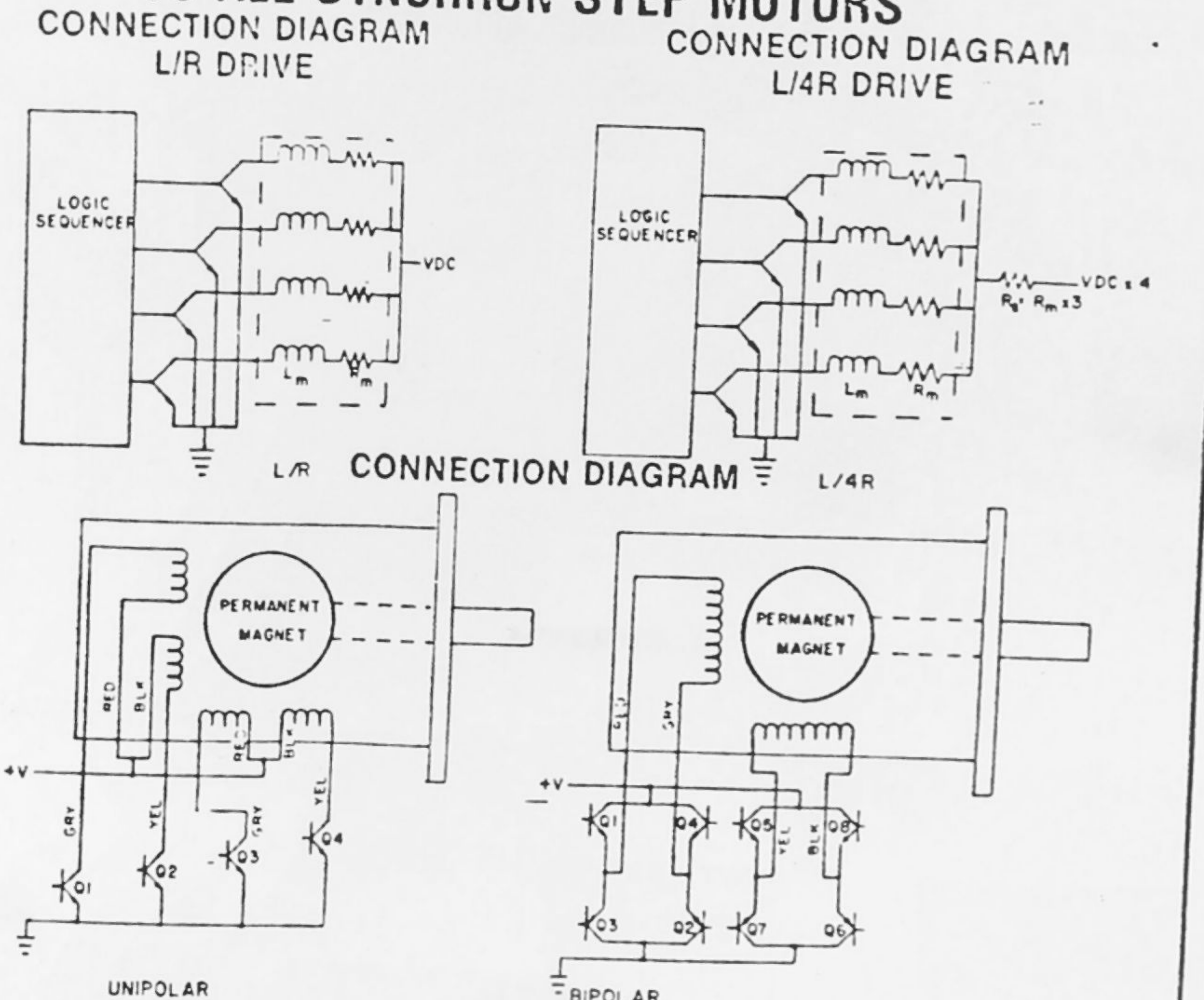
For applications requiring load currents of 1A or less (2A peak), the economical Type UDN-2952B-2 and UDN-2952W-2 are recommended. The lower-cost devices are identical to the basic parts, except for the maximum allowable load-current rating.

These monolithic integrated circuits have extensive circuit protection. Both drivers have thermal shutdown networks that disable motor drive if the package power dissipation ratings are exceeded. Internal diode transient suppression is provided on-chip. Output-current limiting is determined by the user's selection of a sensing resistor.

The Type UDN-2952B full-bridge power driver is supplied in a 16-pin dual in-line plastic package with copper heat-sink contact tabs. The lead configuration enables easy attachment of a heat sink while fitting a standard integrated circuit socket or printed wiring board layout. Type UDN-2952W, for higher power requirements, is in a 12-pin single in-line power tab package. The tab is at ground potential and needs no insulation. For output currents above 700 mA at normal ambient temperatures, both drivers require an external heat sink.

Figure A-14: SPRAGUE : UDN-2952W

EXCITATION CONFIGURATION COMMON TO ALL SYNCHRON STEP MOTORS



SWITCHING SEQUENCE

1 PHASE EXCITATION

STEP	Q1	Q2	Q3	Q4
1	1	0	0	0
2	0	0	0	1
3	0	1	0	0
4	0	0	1	0
1	1	0	0	0

STEP	Q1,Q2	Q3,Q4	Q5,Q6	Q7,Q8
1	1	0	0	0
2	0	0	0	1
3	0	1	0	0
4	0	0	1	0
1	1	0	0	0

2 PHASE EXCITATION

CW ROTATION

1	1	0	1	0
2	1	0	0	1
3	0	1	0	1
4	0	1	1	0
1	1	0	1	0

CCW ROTATION

1	1	0	1	0
2	1	0	0	1
3	0	1	0	1
4	0	1	1	0
1	1	0	1	0

HALF-STEP EXCITATION

1	1	0	1	0
2	1	0	0	0
3	1	0	0	1
4	0	0	0	1
5	0	1	0	1
6	0	1	0	0
7	0	1	1	0
8	0	0	1	0
1	1	0	1	0

1	1	0	1	0
2	1	0	0	0
3	1	0	0	1
4	0	0	0	1
5	0	1	0	1
6	0	1	0	0
7	0	1	1	0
8	0	0	1	0
1	1	0	1	0

Figure A-15: SYNCHRO : STEPPER MOTORS

APPENDIX B

APPENDIX B

B.1 I/O BUS SPECIFICATIONS

HARWARE FREATURE

- External power supply connection
- Directly connected to the data bus
- Addressable I/O block
- Up to 8 I/O interface modules to be connected

INPUT SPECIFICATIONS

- Fully buffered data bus. TTL compatible
- External power supply 5 VDC -5% to +5%
- Interrupt, reset input signal available

OUTPUT SPECIFICATIONS

- 8 selectable I/O range via minijumper

- TTL compatible

- 02, R/W signals available

B.2 UNIVERSAL INTERFACE MODULE

HARDWARE FEATURES

- Eight opto-isolated digital monitoring channels
- Eight forms A relay outputs
- On-board transient protection circuitry

INPUT SPECIFICATIONS

- Eight opto-isolated digital input channels
- Minimum input isolation : 300 volts
- Maximum continuous input voltage : 24 volts
- Two opto-isolated handshake input signals
- Minimum input isolation : 300 volts
- Maximum input voltage : 5 volts

OUTPUT SPECIFICATIONS

- Maximum switching : 30 volts DC or 120 volts AC =
  0.5 amperes

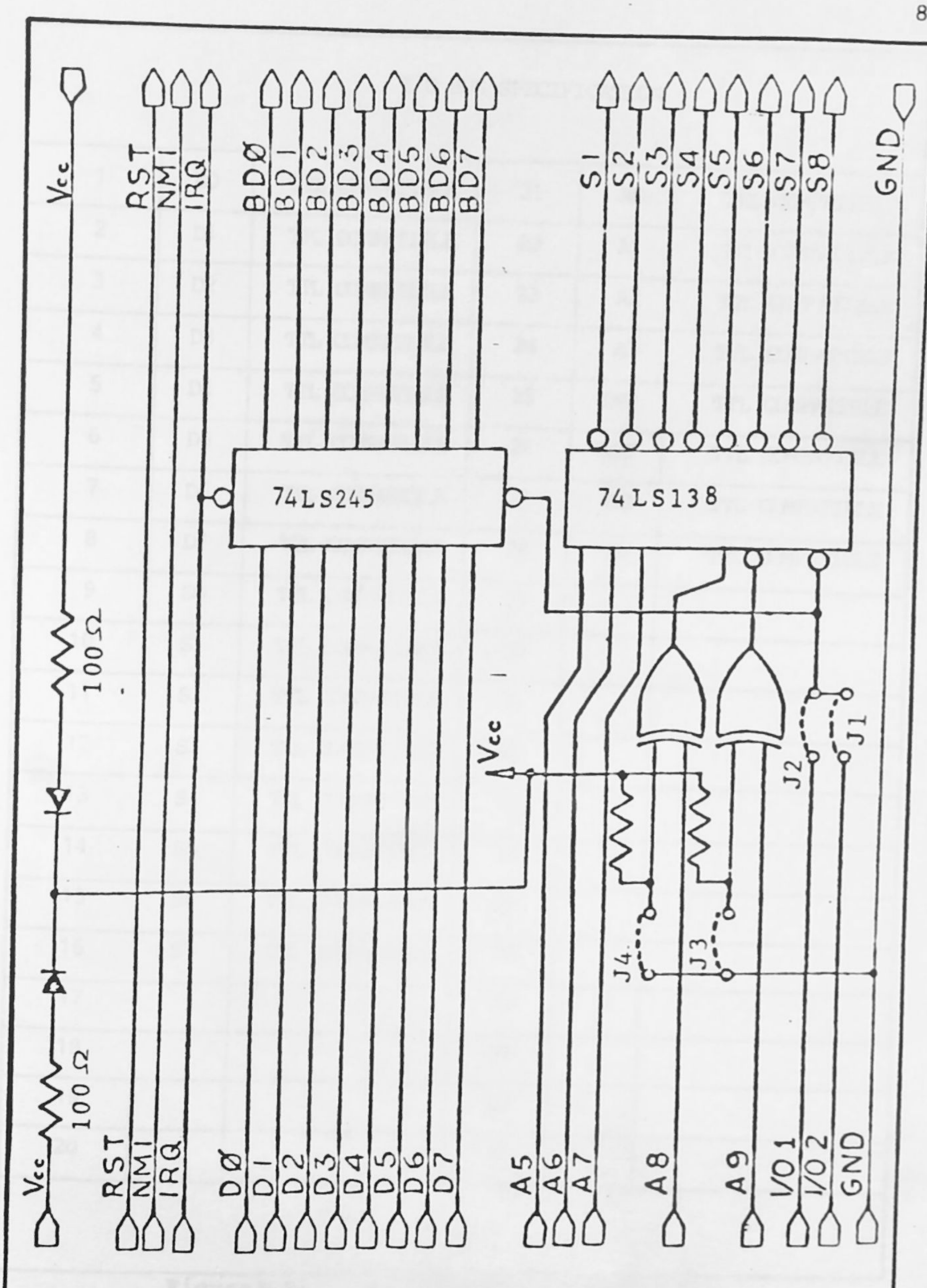


Figure B-1 : I/O BUS EXPANSION MODULE

I/O BUS SPECIFICATION					
1	DO	TTL COMPATIBLE	21	AO	TTL COMPATIBLE
2	D1	TTL COMPATIBLE	22	A1	TTL COMPATIBLE
3	D2	TTL COMPATIBLE	23	A2	TTL COMPATIBLE
4	D3	TTL COMTITIBLE	24	A3	TTL COMPATIBLE
5	D4	TTL COMPATIBLE	25	INT	TTL COMPATIBLE
6	D5	TTL COMPATIBLE	26	RST	TTL COMPATIBLE
7	D6	TTL COMPATIBLE	27	O2	TTL COMPATIBLE
8	D7	TTL COMPATIBLE	28	RW	TTL COMPATIBLE
9	SO	TTL COMPATIBLE	29		
10	S1	TTL COMPATIBLE	30		
11	S2	TTL COMPATIBLE	31		
12	S3	TTL COMPATIBLE	32		
13	S4	TTL COMPATIBLE	33		
14	S5	TTL COMPATIBLE	34		
15	S6	TTL COMPATIBLE	35		
16	S7	TTL COMPATIBLE	36		
17			37		
18			38		
19			39		
20			40		

Figure B-2: I/O BUS SPECIFICATIONS

10 VA resistive

- Minimum isolation : 300 volts

  transient protectors (Tranzorbs) are

  provided for reactive loads

- Two opto-isolated handshake output signals

- Minimum isolation : 300 volts

- Maximum switching voltage : 30 volts DC (100 mA)

B.3 STEPPER MOTOR INTERFACE (INPUTS)

HARDWARE FEATURES

- 16 opto-isolated digital monitoring channels

- TTL compatible

- On-board transient protection circuitry

INPUT SPECIFICATIONS

- 16 opto-isolated digital input channels

- Minimum input isolation : 300 volts

- Maximum continuous input voltage : 24 volts

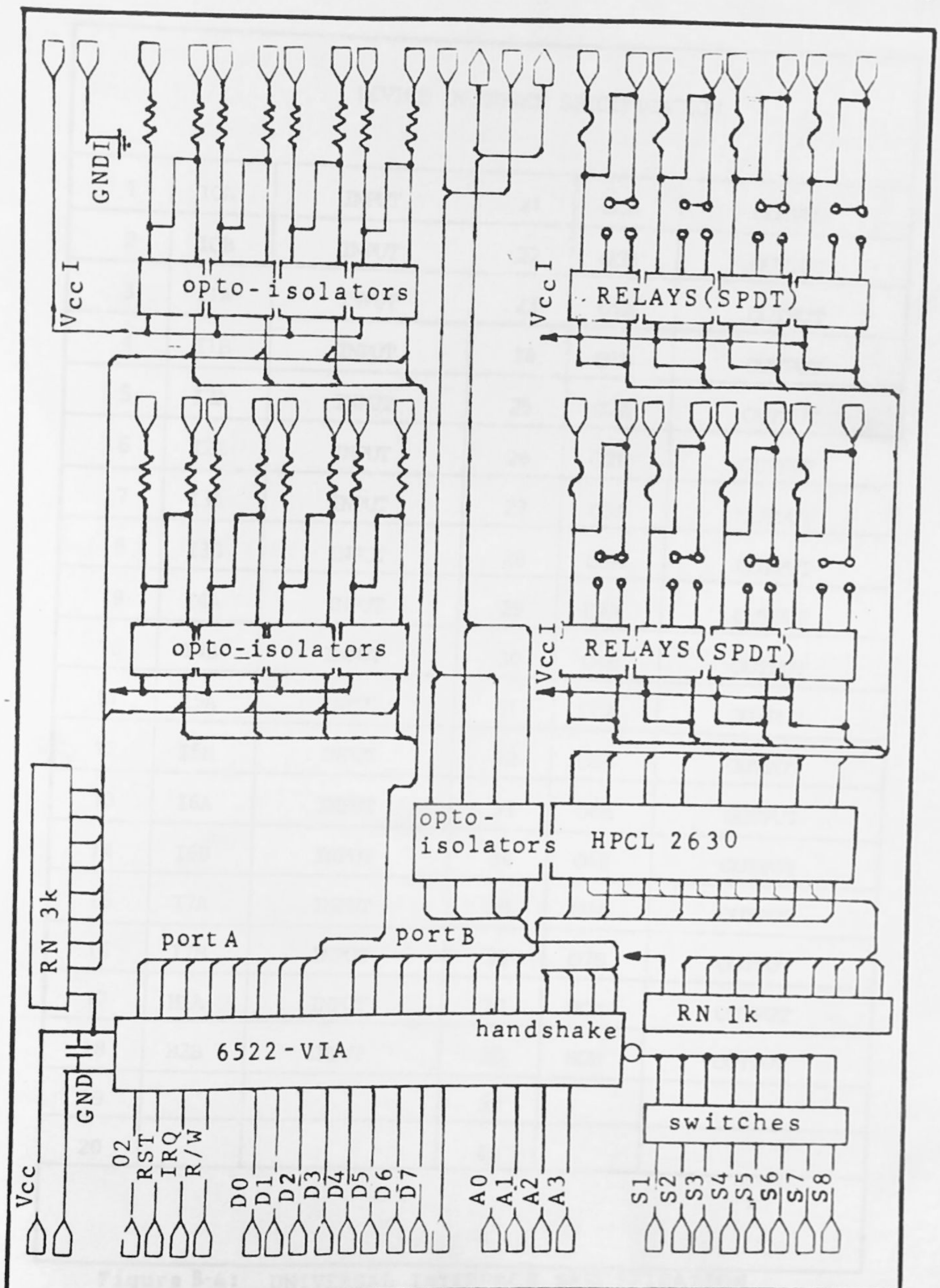


Figure B-3: UNIVERSAL INTERFACE MODULE

DEVICE INTERFACE SPECIFICATION					
1	IOA	INPUT	21	OOA	OUTPUT
2	IOB	INPUT	22	OOB	OUTPUT
3	I1A	INPUT	23	O1A	OUTPUT
4	I1B	INPUT	24	O1B	OUTPUT
5	I2A	INPUT	25	O2A	OUTPUT
6	I2B	INPUT	26	O2B	OUTPUT
7	I3A	INPUT	27	O3A	OUTPUT
8	I3B	INPUT	28	O3B	OUTPUT
9	I4A	INPUT	29	O4A	OUTPUT
10	I4B	INPUT	30	O4B	OUTPUT
11	I5A	INPUT	31	O5A	OUTPUT
12	I5B	INPUT	32	O5B	OUTPUT
13	I6A	INPUT	33	O6A	OUTPUT
14	I6B	INPUT	34	O6B	OUTPUT
15	I7A	INPUT	35	O7A	OUTPUT
16	I7B	INPUT	36	O7B	OUTPUT
17	HIA	INPUT	37	HOA	OUTPUT
18	H2B	INPUT	38	HOB	OUTPUT
19			39		
20			40		

Figure B-4: UNIVERSAL INTERFACE SPECIFICATION

- Minimum input voltage : 0 volts

B.4 STEPPER MOTOR INTERFACE (OUTPUTS)

HARDWARE FEATURES

- 16 Binary output channels
- TTL compatible

OUTPUT SPECIFICATIONS

- Maximum switching : 30 volts DC
  100 mA
- Minimum isolation : 300 volts

B.5 DC MOTOR INTERFACE MODULE

HARDWARE FEATURES

- Eight analog output channels
- Seven bits resolution
- Industry standard voltage or current input
- On-board transient protection circuitry

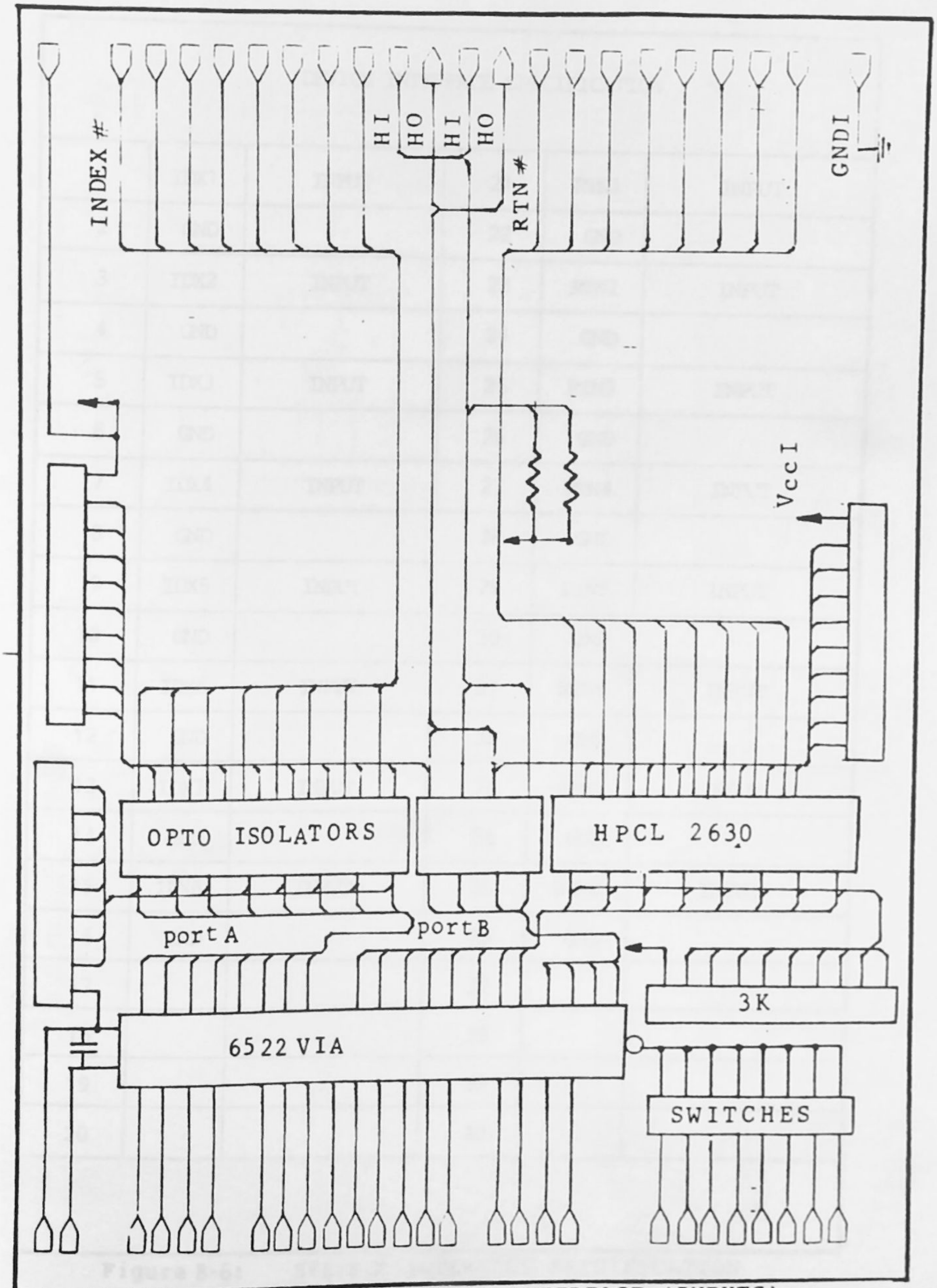


Figure B-5: STEPPER MOTOR INTERFACE (INPUTS)

DEVICE INTERFACE SPECIFICATION					
1	IDX1	INPUT	21	RTN1	INPUT
2	GND		22	GND	
3	IDX2	INPUT	23	RTN2	INPUT
4	GND		24	GND	
5	IDX3	INPUT	25	RTN3	INPUT
6	GND		26	GND	
7	IDX4	INPUT	27	RTN4	INPUT
8	GND		28	GND	
9	IDX5	INPUT	29	RTN5	INPUT
10	GND		30	GND	
11	IDX6	INPUT	31	RTN6	INPUT
12	GND		32	GND	
13	IDX7	INPUT	33	RTN7	INPUT
14	GND		34	GND	
15	IDX8	INPUT	35	RTN8	INPUT
16	GND		36	GND	
17			37		
18			38		
19			39		
20			40		

Figure B-6: STEPPER INTERFACE SPECIFICATION

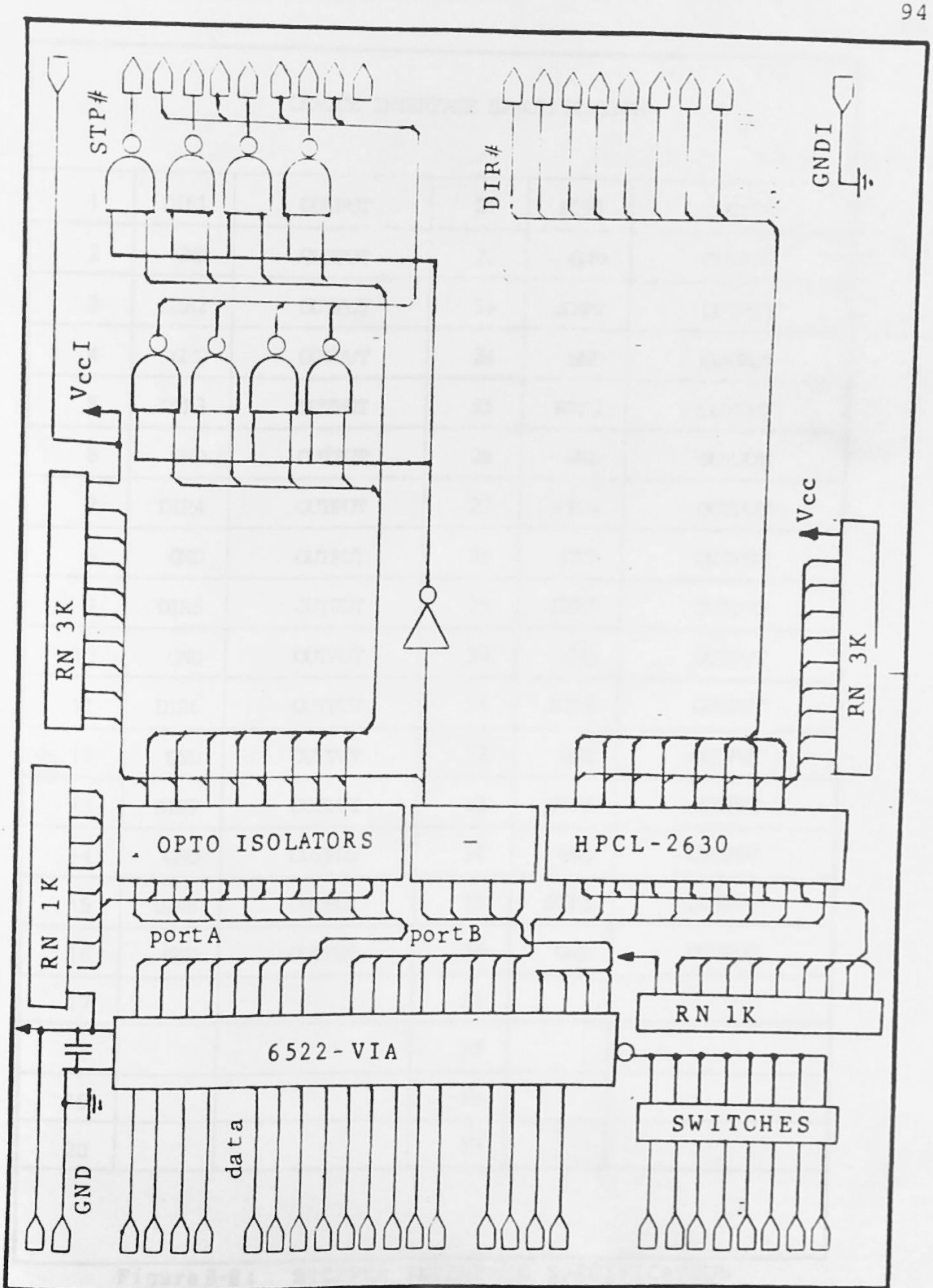


Figure B-7: STEPPER MOTOR INTERFACE (OUTPUTS)

DEVICE INTERFACE SPECIFICATION

1	DIR1	OUTPUT	21	STP1	OUTPUT
2	GND	OUTPUT	22	GND	OUTPUT
3	DIR2	OUTPUT	23	STP2	OUTPUT
4	GND	OUTPUT	24	GND	OUTPUT
5	DIR3	OUTPUT	25	STP3	OUTPUT
6	GND	OUTPUT	26	GND	OUTPUT
7	DIR4	OUTPUT	27	STP4	OUTPUT
8	GND	OUTPUT	28	GND	OUTPUT
9	DIR5	OUTPUT	29	STP5	OUTPUT
10	GND	OUTPUT	30	GND	OUTPUT
11	DIR6	OUTPUT	31	STP6	OUTPUT
12	GND	OUTPUT	32	GND	OUTPUT
13	DIR7	OUTPUT	33	STP7	OUTPUT
14	GND	OUTPUT	34	GND	OUTPUT
15	DIR8	OUTPUT	35	STP8	OUTPUT
16	GND	OUTPUT	36	GND	OUTPUT
17			37		
18			38		
19			39		
20			40		

Figure B-8: STEPPER INTERFACE SPECIFICATION

- Optically Isolated Interface
  between processor and driver modules

OUTPUT SPECIFICATIONS

- isolated output channels
- Output ranges : 0 to Vpp (up to 28 VDC)
- Resolution : 7 -bits binary
- Accuracy : relative -1/4 or +1/4 LSB
  fullscale -1 or +1 LSB
  Zero error -1 or +1 LSB
- Power Supply Range : Vcc = 5 VDC, Vpp = 5 to 30 VDC
- Compliance Voltage : (power supply voltage) -10 volts
- Isolation : 300 volts

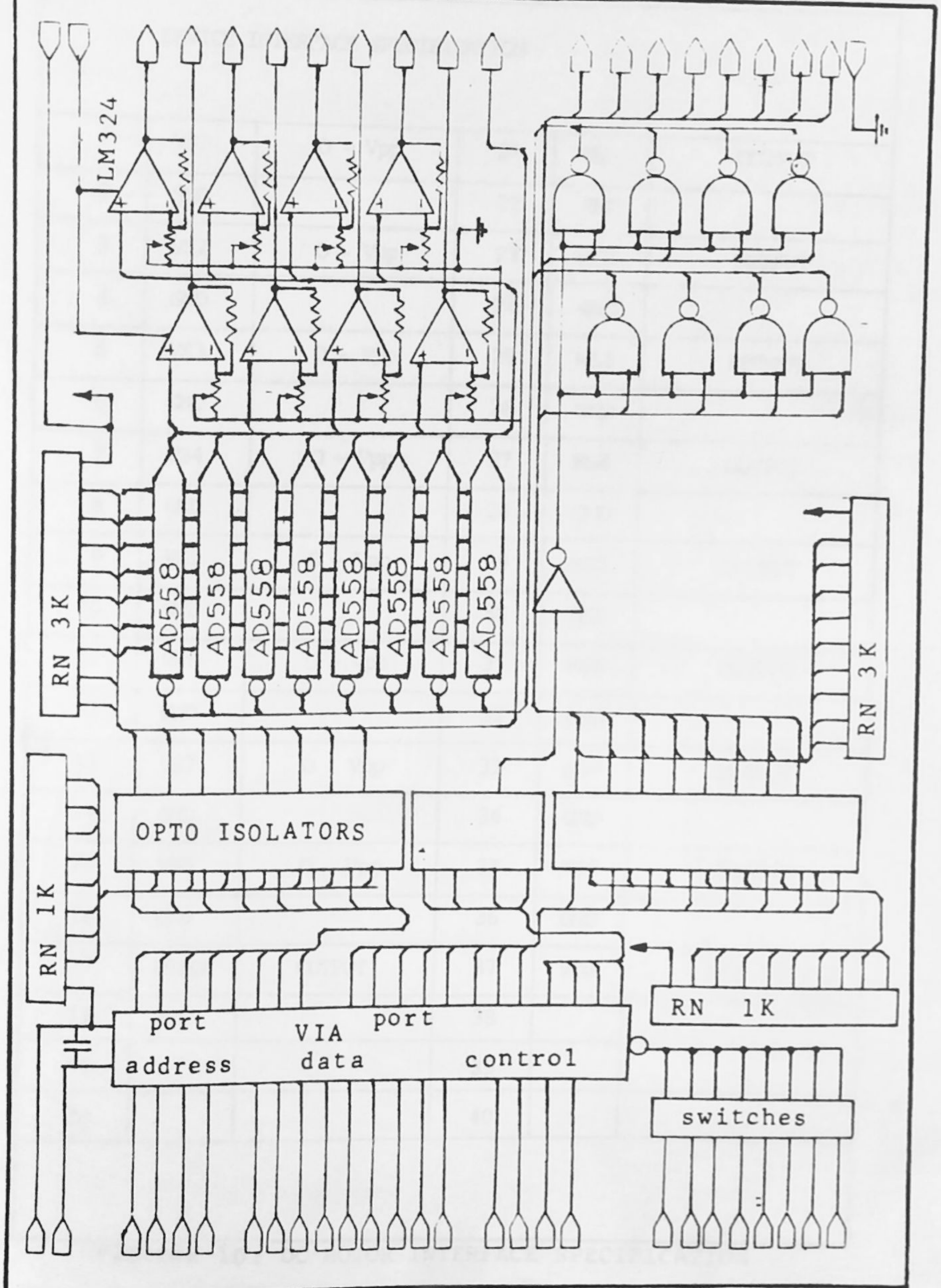


Figure B-9: DC MOTOR INTERFACE MODULE

DEVICE INTERFACE SPECIFICATION					
1	VS1	O - Vpp	21	MS1	OUTPUT
2	GND		22	GND	
3	VS2	O - Vpp	23	MS2	OUTPUT
4	GND		24	GND	
5	VS3	O - Vpp	25	MS3	OUTPUT
6	GND		26	GND	
7	VS4	O - Vpp	27	MS4	OUTPUT
8	GND		28	GND	
9	VS5	O - Vpp	29	MS5	OUTPUT
10	GND		30	GND	
11	VS6	O - Vpp	31	MS6	OUTPUT
12	GND		32	GND	
13	VS7	O - Vpp	33	MS7	OUTPUT
14	GND		34	GND	
15	VS8	O - Vpp	35	MS8	OUTPUT
16	GND		36	GND	
17	MTRON	OUTPUT	37	Vpp	O - 30 VDC
18	GND		38		
19			39		
20			40		

Figure B-10: DC MOTOR INTERFACE SPECIFICATION

B.6 ANALOG INPUTS INTERFACE MODULE

HARDWARE FREATURES

- Two groups of 8 single-ended analog monitoring channels
- Seven bit resolution
- Industry standard voltage or current input
- Integrating inputs for optimum power line noise rejection
- Each channel converted every 400 microseconds
- On-board transient protection circuitry
- Optically Isolated Interface

  between processor and analog to digital converter DAS-952R

INPUT SPECIFICATIONS

- 16 single-ended input channels
- Input range : 0-5 VDC, 0-20mA
- Resolution : 8-bits binary
- Accuracy : 7-bits binary
- Temperature Coefficient of Accuracy

  Voltage Range : -0.003% or +0.003% per Degree C

  Current Range : -0.008% per Degree C

- Common Mode Rejection Ratio : 86 dB
- Voltage Input Configuration

maximum common mode input voltage :

5 volts for maximum accuracy

30 volts without damage

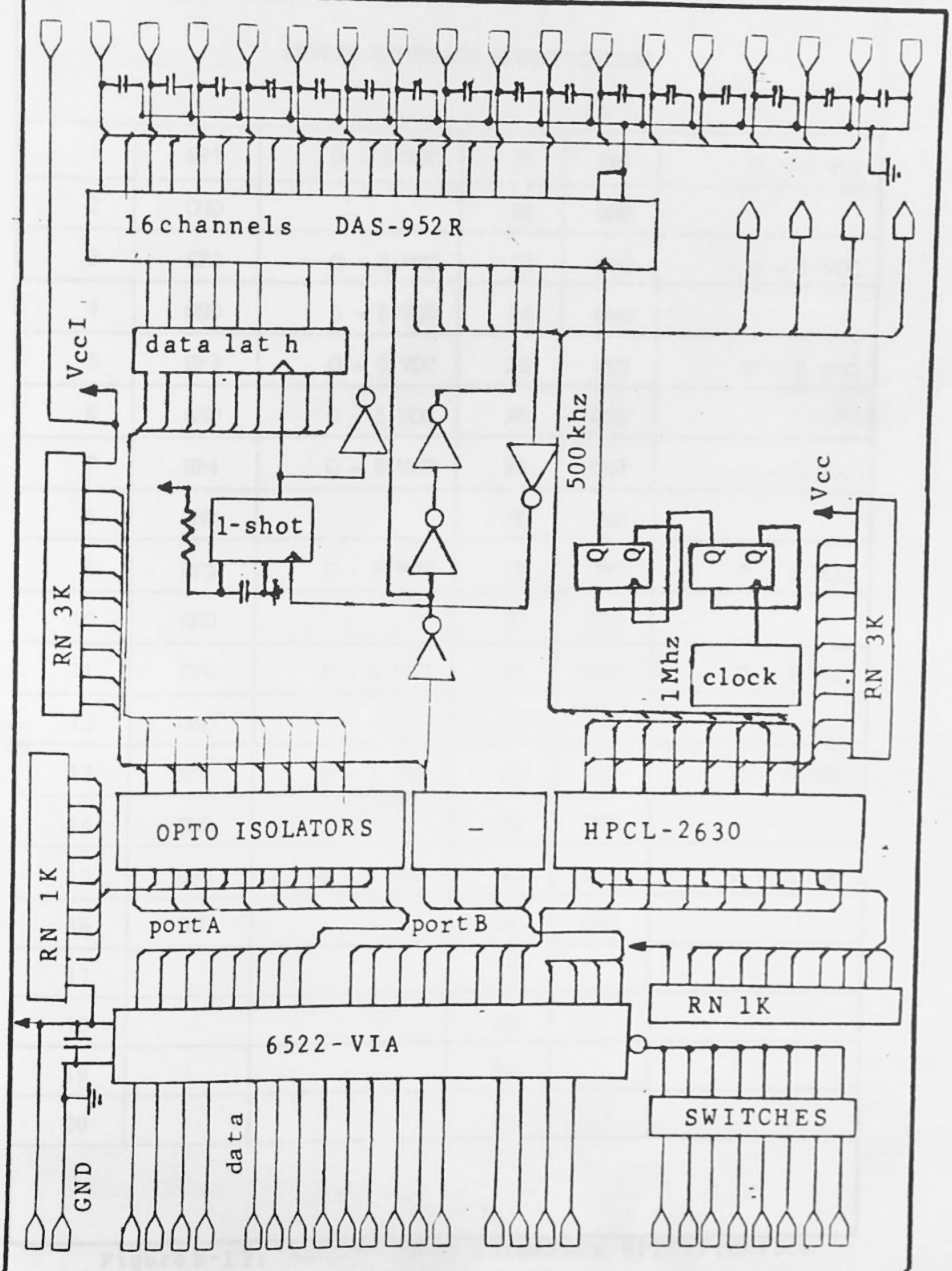
B.7 STEPPER MOTOR DRIVER MODULE A/B

HARDWARE FEATURES

- Programmable stepping rate
- Fullwave drive
- Module A for bipolar drive
- Module B for unipolar chopper drive
- Up to 0.5 A per phase
- Up to 30 VDC supply
- On board protection circuitry

INPUT SPECIFICATIONS

- TTL compatible inputs
- External power supply up to 30 VDC



FigureB-11: ANALOG INPUT INTERFACE MODULE

DEVICE INTERFACE SPECIFICATION					
1	SP1	0 - 5 VDC	21	CH1	0 - 5 VDC
2	GND		22	GND	
3	SP2	0 - 5 VDC	23	CH2	0 - 5 VDC
4	GND	0 - 5 VDC	24	GND	
5	SP3	0 - 5 VDC	25	CH3	0 - 5 VDC
6	GND	0 - 5 VDC	26	GND	
7	SP4	0 - 5 VDC	27	CH4	0 - 5 VDC
8	GND		28	GND	
9	SP5	0 - 5 VDC	29	CH5	0 - 5 VDC
10	GND		30	GND	
11	SP6	0 - 5 VDC	31	CH6	0 - 5 VDC
12	GND		32	GND	
13	SP7	0 - 5 VDC	33	CH7	0 - 5 VDC
14	GND		34	GND	
15	SP8	0 - 5 VDC	35	CH8	0 - 5 VDC
16	GND		36	GND	
17			37		
18			38		
19			39		
20			40		

Figure B-12: ANALOG INPUT INTERFACE SPECIFICATION

OUTPUT SPECIFICATIONS

- module A : up to 0.5 A per phase
- module B : up to 0.5 A per phase
- chopper output voltage available

B.8 DC MOTOR DRIVER MODULE

HARDWARE FEATURES

- Programmable speed range
- Current feedback for stability
- Dynamic braking
- Motorjam detection
- On board protection circuitry
- Up to 5 A surge current
- Stop and start operation

INPUT SPECIFICATIONS

- Analog input for speed control (0 to 30 VDC)
- External power supply up to 30 VDC

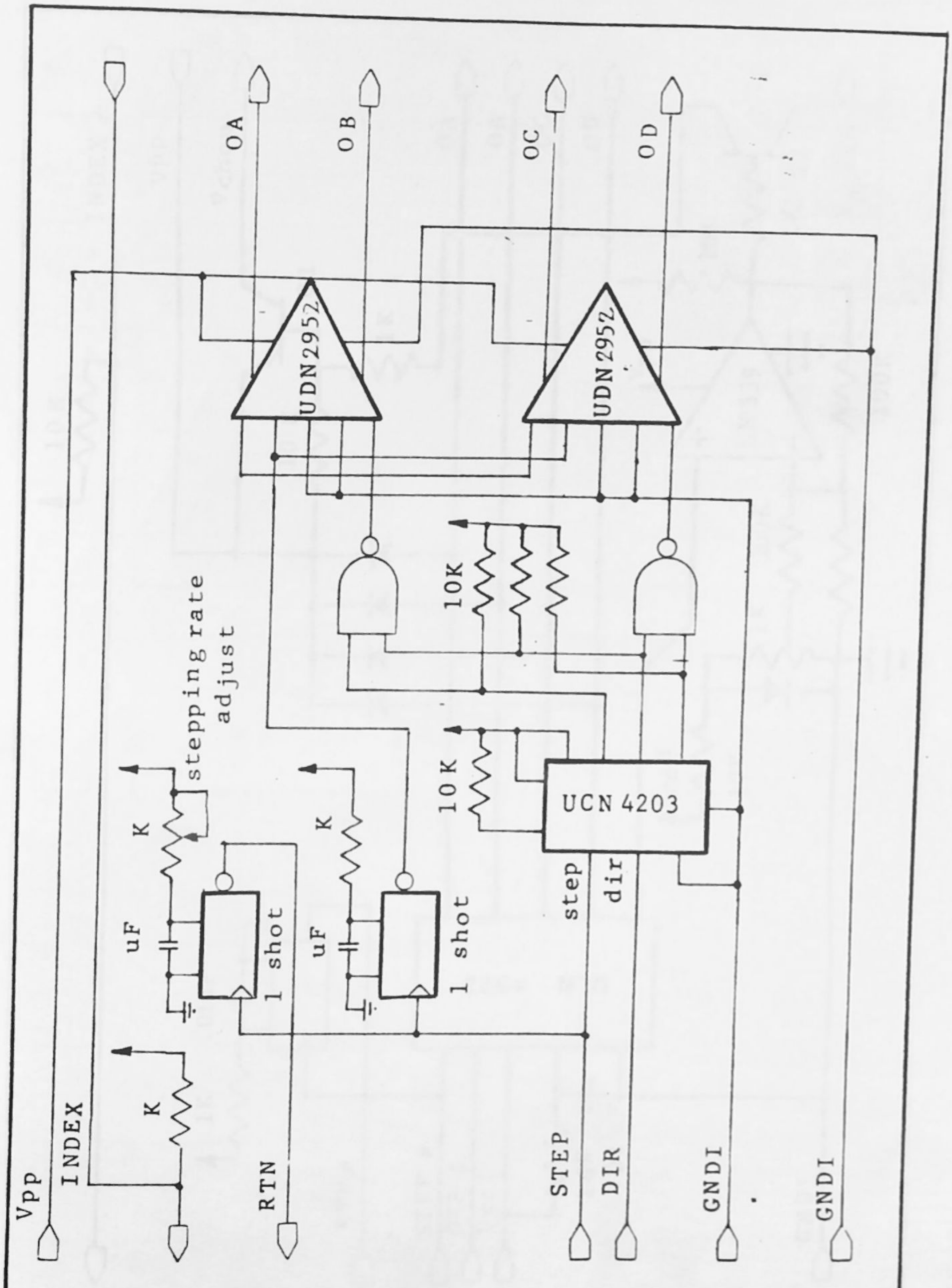


Figure B-13: STEPPER MOTOR DRIVER MODULE A

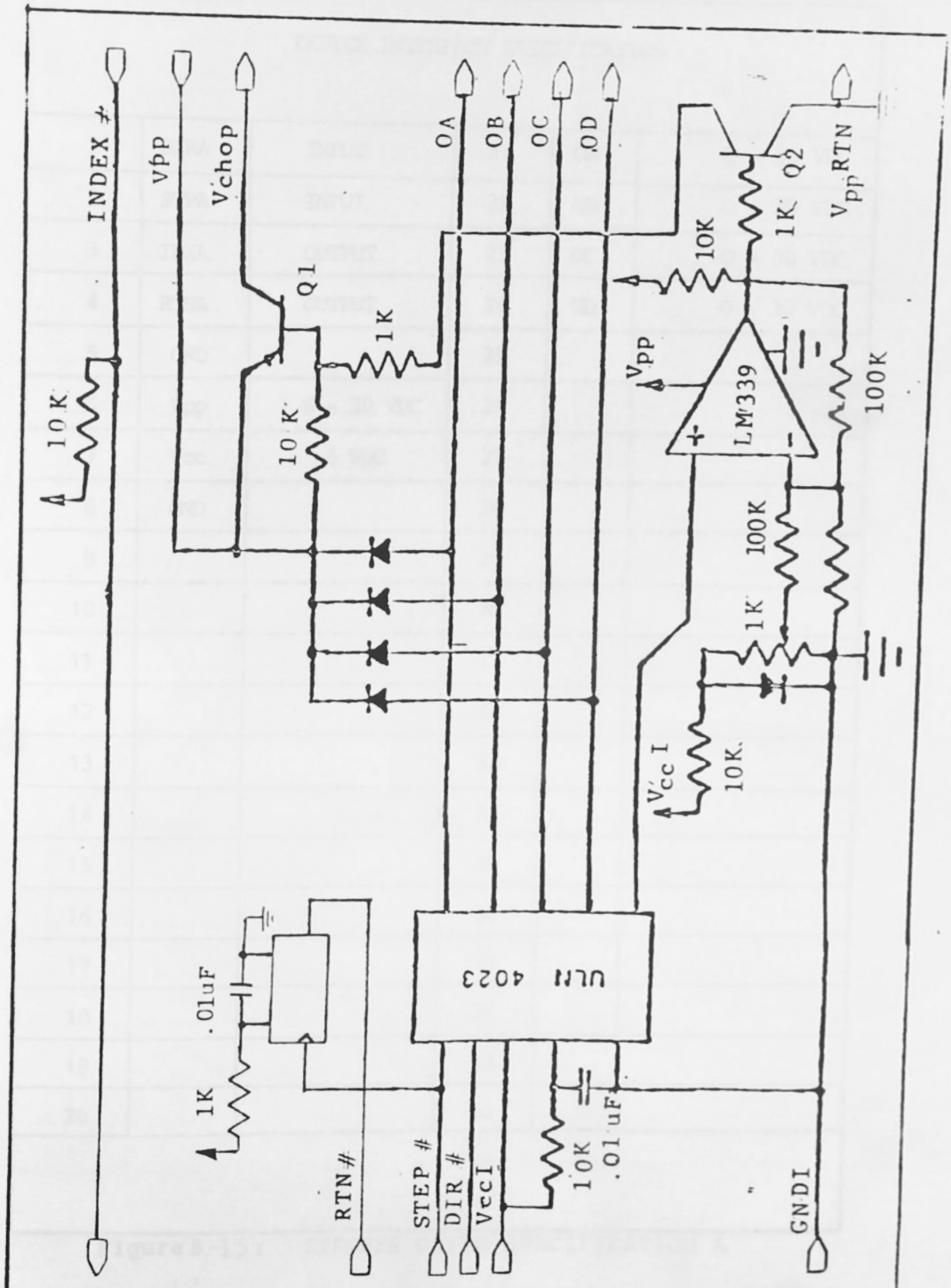


Figure B-14: STEPPER MOTOR DRIVER MODULE B ER CIRCUIT

DEVICE INTERFACE SPECIFICATION

1	DIRA	INPUT	21	OA	O - 30 VDC
2	STPA	INPUT	22	OB	O - 30 VDC
3	IDXA	OUTPUT	23	OC	O - 30 VDC
4	RTNA	OUTPUT	24	OD	O - 30 VDC
5	GND		25		
6	Vpp	6 - 30 VDC	26		
7	Vcc	5 VDC	27		
8	GND		28		
9			29		
10			30		
11			31		
12			32		
13			33		
14			34		
15			35		
16			36		
17			37		
18			38		
19			39		
20			40		

Figure B-15: STEPPER DRIVE SPECIFICATION A

DEVICE INTERFACE SPECIFICATION

1			21		
2			22		
3			23		
4	--		24		
5			25		
6			26		
7			27		
8			28		
9			29		
10			30		
11	DIRB	INPUT	31	OA	0 - 30 VDC
12	STPB	INPUT	32	OB	0 - 30 VDC
13	IDXB	INPUT	33	OC	0 - 30 VDC
14	RTNB	OUTPUT	34	OD	0 - 30 VDC
15	GND		35	Vchop	0 - 30 VDC
16	Vpp	6 - 30 VDC	36		0 - 30 VDC
17	Vcc	5 VDC	37		
18	GND		38		
19			39		
20			40		

Figure B-16: STEPPER DRIVE SPECIFICATION B

- TTL compatible control input

OUTPUT SPECIFICATIONS

- Up to 5A/30 VDC
- TTL compatible motor jammed output

B.9 SPEED SENSING MODULE

HARDWARE FEATURES

- To be used with photo sensing or
  hall effect sensing
- Dynamic threshold control
- Adjustable frequency input range
- Adjustable output voltage range
- TTL compatible
- Frequency output

INPUT SPECIFICATIONS

- Analog input : 0-5 VDC
- Common mode rejection radio : 86 dB

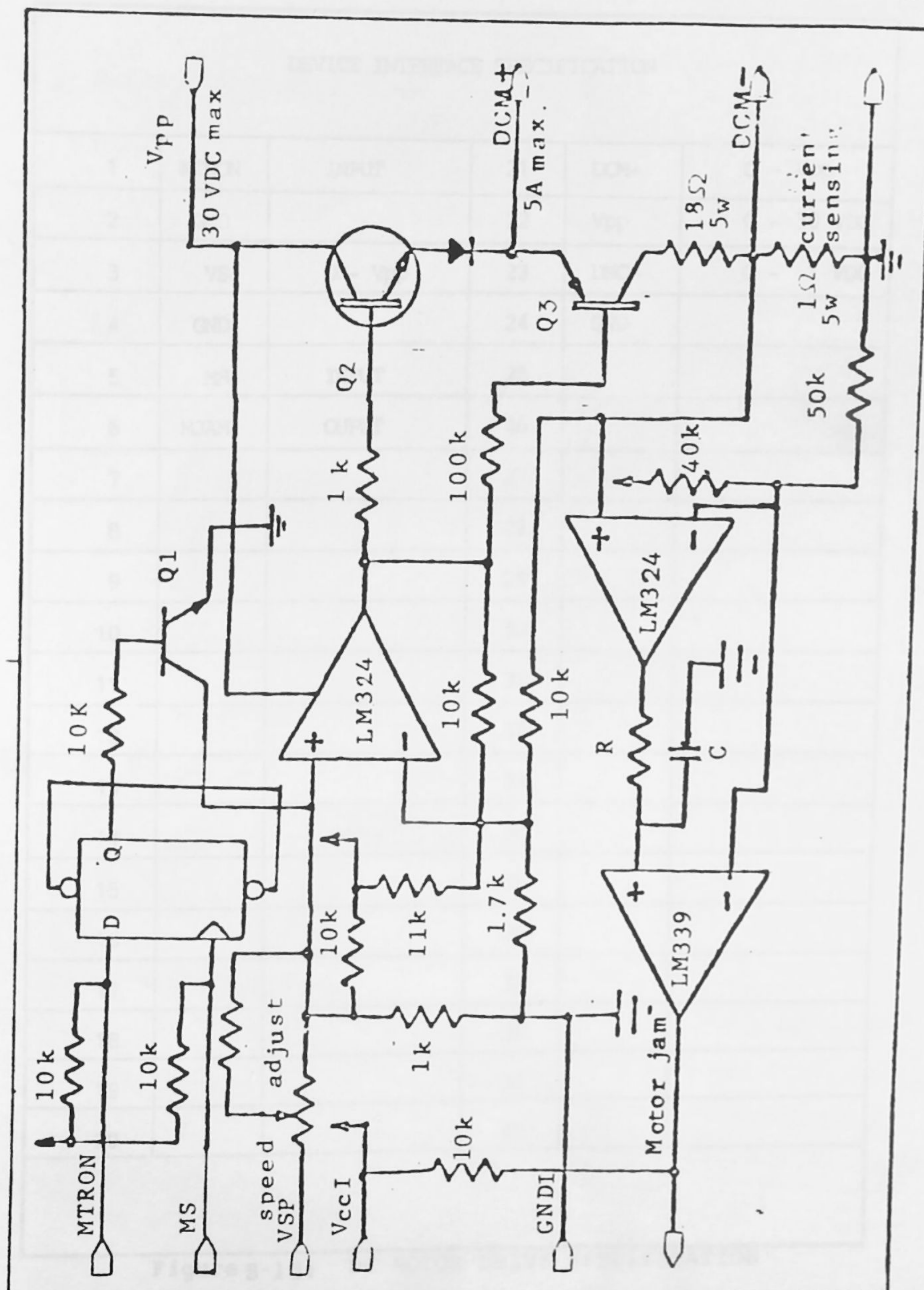


Figure B-17: DC MOTOR DRIVER MODULE

DEVICE INTERFACE SPECIFICATION

1	MTRON	INPUT	21	DCM+	O - Vpp
2	GND		22	Vpp	O - 30 VDC
3	VS	O - Vpp	23	DMC-	O - 1 VDC
4	GND		24	GND	
5	MS	INPUT	25		
6	MJAM	OUPUT	26		
7			27		
8			28		
9			29		
10			30		
11			31		
12			32		
13			33		
14			34		
15			35		
16			36		
17			37		
18			38		
19			39		
20			40		

Figure B-18: DC MOTOR DRIVE SPECIFICATION

- Maximum frequency range : 5 kHZ
- Minimum frequency range : 0 HZ

OUTPUT SPECIFICATIONS

- Analog output : 0-5 VDC, 0-20 mA

B.10 INPUT CONDITIONING MODULE

HARDWARE FEATURE

- AC or DC measurements
- Full wave rectified AC inputs
- Scaling for high input voltages
- On board transient protection

INPUT SPECIFICATIONS

- Analog input : 0-30 V (AC or DC)
- Common mode rejection ratio : 86 dB

OUTPUT SPECIFICATIONS

- Analog output : 0-5 VDC, 0-20 mA

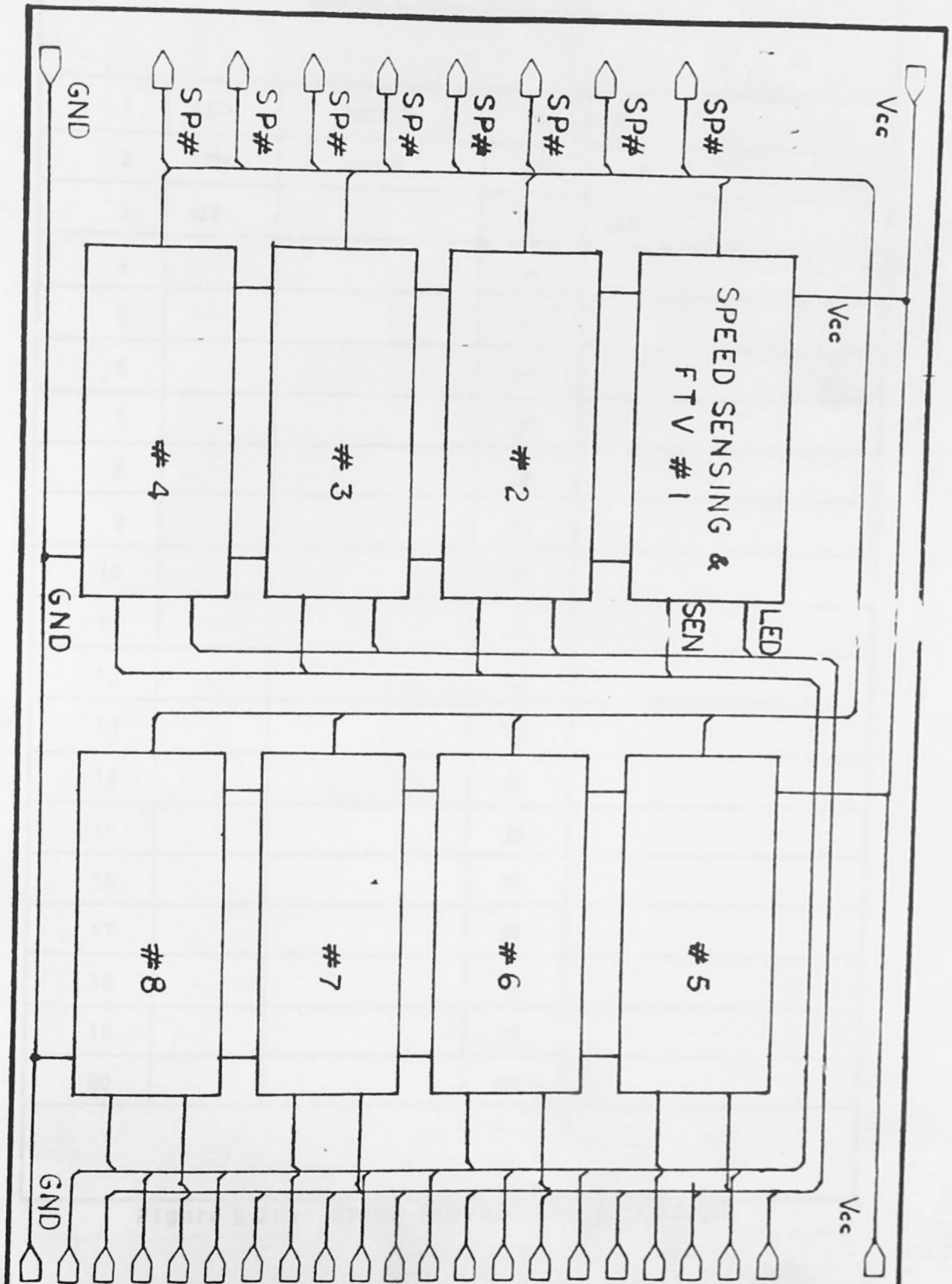


Figure B-19: SPEED SENSING MODULE

DEVICE INTERFACE SPECIFICATION

1	LED	OUTPUT	21	Vcc	+5VDC
2	SEN	INPUT	22	SP#	0 - 5 VDC
3	GND		23	GND	
4			24		
5			25		
6			26		
7			27		
8			28		
9			29		
10			30		
11			31		
12			32		
13			33		
14			34		
15			35		
16			36		
17			37		
18			38		
19			39		
20			40		

Figure B-20: SPEED SENSING SPECIFICATION

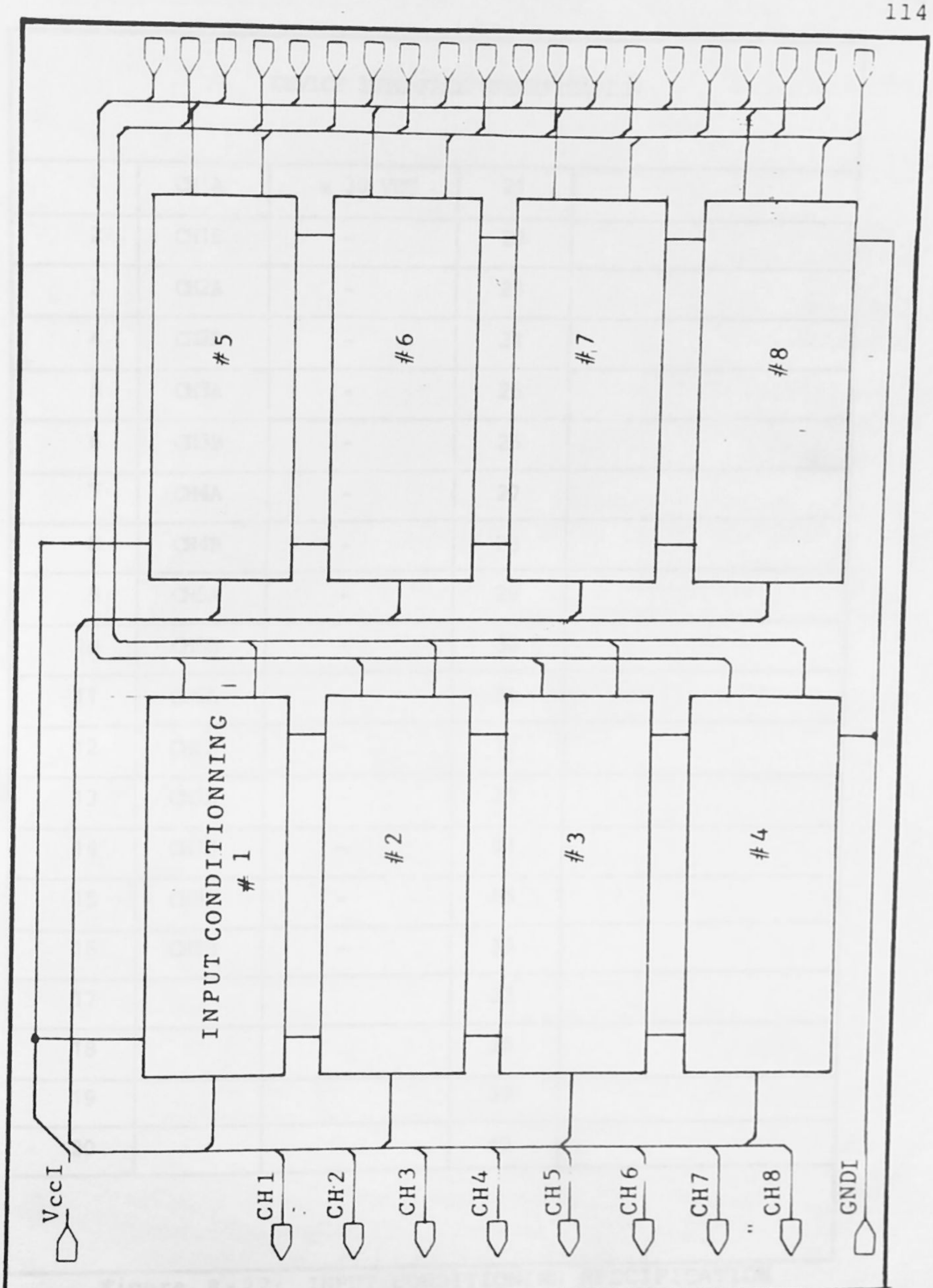


Figure B-21: INPUT CONDITIONING MODULE

DEVICE INTERFACE SPECIFICATION

1	CH1A	± 30 VDC	21	
2	CH1B	-	22	
3	CH2A	-	23	
4	CH2B	-	24	
5	CH3A	-	25	
6	CH3B	-	26	
7	CH4A	-	27	
8	CH4B	-	28	
9	CH5A	-	29	
10	CH5B	-	30	
11	CH6A	-	31	
12	CH6B	-	32	
13	CH7A	-	33	
14	CH7B	-	34	
15	CH8A	-	35	
16	CH8B	-	36	
17			37	
18			38	
19			39	
20			40	

Figure B-22: INPUT CONDITIONING SPECIFICATION

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